INSTRUCTION MANUAL

FOR

WJ-8718/232 OPTION

WATKINS-JOHNSON

INSTRUCTION MANUAL

FOR

WJ-8718/232 OPTION

The WJ-8718/232 Option Instruction Manual supplements the WJ-8718 HF Receiver Instruction Manual and is to be used in conjunction with that manual.

WATKINS-JOHNSON COMPANY
700 QUINCE ORCHARD ROAD
GAITHERSBURG, MARYLAND 20878

8/79

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with this equipment with any of the protective covers removed.

WJ-8718/232 OPTION INSTRUCTION MANUAL
CHANGE 1

TITLE: INSTRUCTION MANUAL FOR WJ-8718/232 OPTION

MANUAL DATE: AUGUST 1979

CHANGE 1 DATE: SEPTEMBER 1990

APPLICABILITY: All WJ-8718 Receivers with the WJ-8718/232 Option.

CHANGES/ERRATA INFORMATION: Changes refer to updates of the manual to cover design modifications. Errata refer to corrections or clarifications of information in the manual.

CHANGE SUMMARY: This change corrects erroneous information in the manual relative to selection of the baud rate for the RS-232C interface.

ERRATA:

Page 1-8 Delete **Table 1-2** and replace with the table shown below:

Table 1-2. Baud Rate Codes

Baud Rate	S1-4	S1-3	S1-2	S1-1
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
134.5	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2000	1	0	0	1
2400	1	0	1	0
3600	1	0	1	1
4800	1	1	0	0
7200	1	1	0	1
9600	1	1	1	0
19200	1	1	1	1

CHANGES: None

February 15, 1980
ADDENDUM I

The information in this addendum is to be incorporated into paragraph 1.3, Installation Procedures, of the WJ-8718/232 Instruction Manual.

1.1 PURPOSE OF ADDENDUM

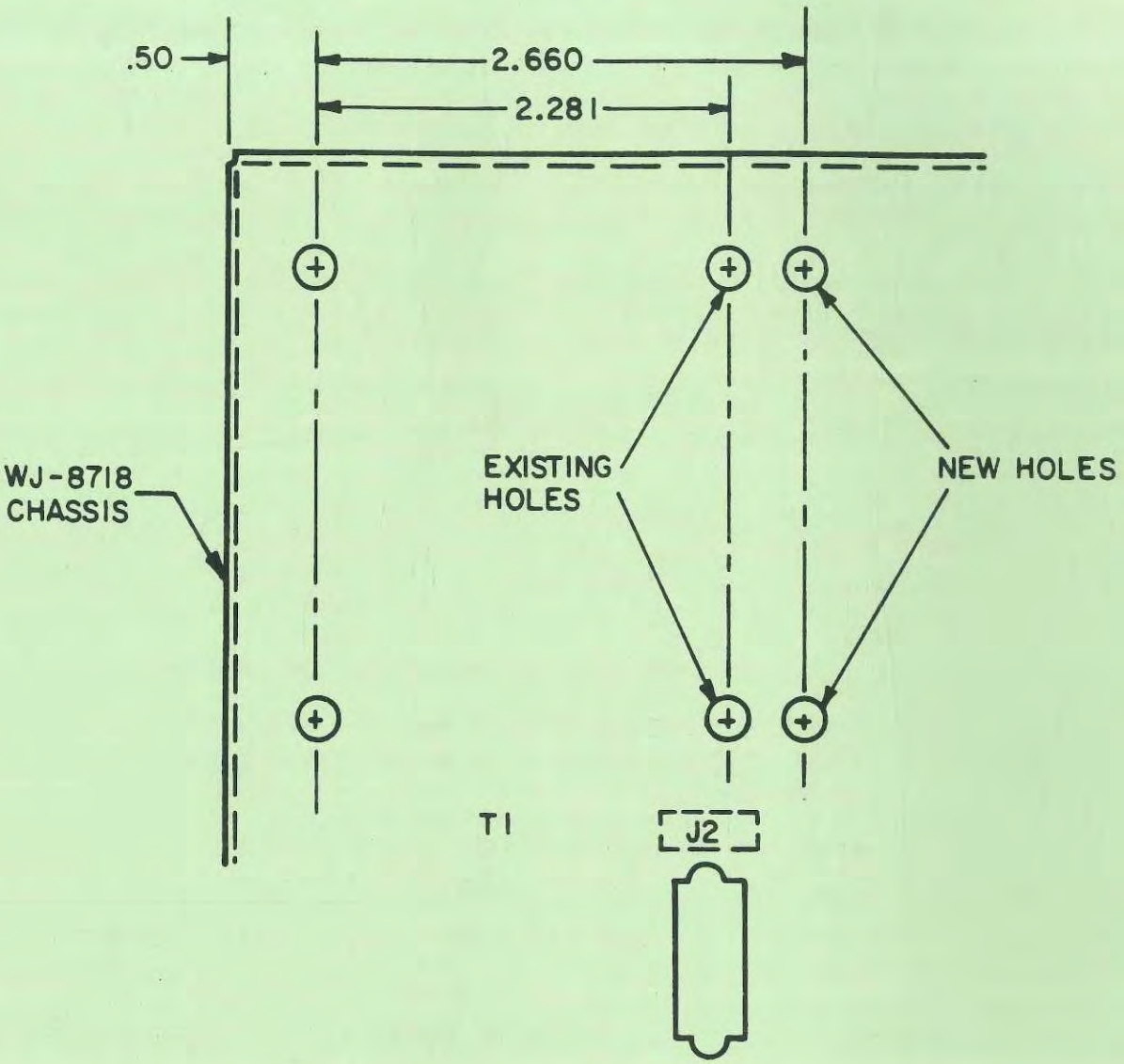
The Type 34518-1 power transformer (T1), installed in many WJ-8718 HF Receivers in the field, does not meet the power requirements of the WJ-8718/232 Option. If such a receiver is to be equipped with the 232 option, it is necessary to replace the transformer with the Type 380083 power transformer, available from Watkins-Johnson, Gaithersburg, Maryland.

1.2 EQUIPMENT REQUIRED

Type 380083 power transformer
#6 lockwashers and nuts (4 each)

1.3 INSTALLATION PROCEDURE

1. Remove power from the receiver.
2. Remove the top and bottom dust covers.
3. Unplug the cable connections to T1.
4. Remove the 4 screws securing T1 to the chassis and remove the transformer from the receiver. Retain the screws for reassembly.
5. Drill two holes in the receiver chassis as shown in the diagram on page 2 of this addendum.
6. Mount the new transformer in the chassis and secure with screws (removed in step 4, above), lockwashers, and nuts.
7. Plug the cables into the transformer as instructed on the wire and transformer labels.
8. Replace the top and bottom dust covers.



Chassis Modification Diagram

May 7, 1980
ADDENDUM II

1.1 PURPOSE OF ADDENDUM

Addendum II directs the attention of the manual user to Appendix I, Product Improvements (page 1-91), of this WJ-8718/232 Option Instruction Manual. The appendix expands the manual format to include information concerning extensive engineering changes to the equipment, occuring after the publication of the instruction manual. Extensive engineering changes are those modifications which require revised schematic diagrams, parts lists, and location of component diagrams. As such changes occur, the appropriate data will be added to Appendix I. Minor manual updates will continue to be addressed by addenda.

1.2 MANUAL REVISIONS

1.2.1 Add the following items to the Table of Contents following PARTS LISTS, Paragraph 1.10.2:

APPENDIX I
PRODUCT IMPROVEMENTS

1.2.2 Add the following items to the List of Illustrations:

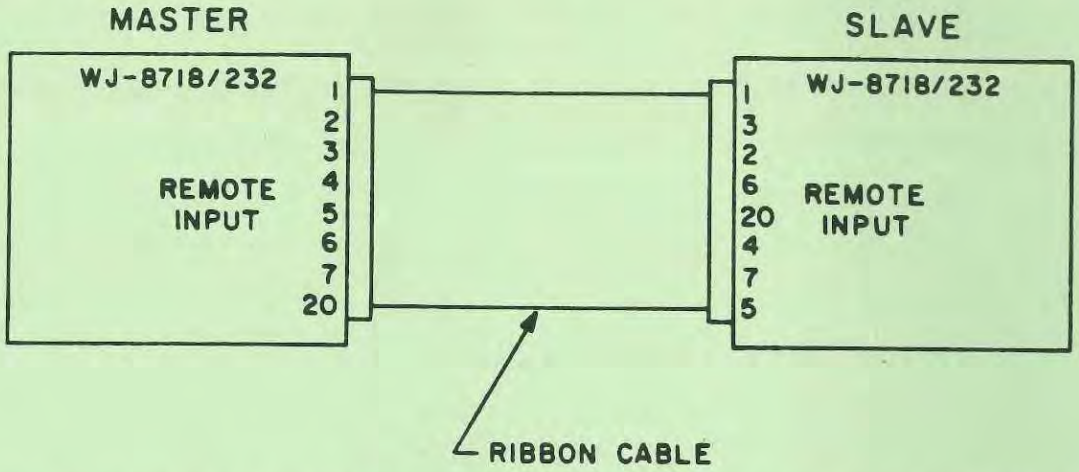
1.2.3 Add the following items to the List of Tables:

May 19, 1980
ADDENDUM III

The information in this addendum is provided to correct and update the WJ-8718/232 Option Instruction Manual.

1.1 Add the following information to paragraph 1.5.1, RS-232-C Interface Bus:

The receiver-to-receiver connections in the daisy chain configuration are pin-for-pin compatible when all are configured as slaves. If two receivers are configured as master and slave (reference paragraph 1.4.4), reverse cable (modem bypass) must be used between the receivers, with pin connections as shown below.



1.2 Correct paragraph 1.6.4.1.2 by changing the reference from Figure 1-5 (in the tenth line) to Figure 1-6.

1.3 Correct Figure 1-9, page 1-29, by changing the components in the ADDRESS DECODE block (to the right of the bus line) from "U5A, U6, U8" to "U5B, U6, U8."

1.4 Correct paragraph 1.7.3.5, page 1-56, by changing the fifth line from "...up to 2 less 1," to "...up to 2^{15} less 1."

1.5 The value and polarity of C13 on the IF Interface (232-A2) has been changed to compensate for increased capacitance on the 10 V line during power up. Change the parts list and schematic diagram as listed below.

1.5.1 Paragraph 1.10.2, page 1-77, Type 796032 parts list, should be corrected as follows:

1. From: C13, Capacitor, Ceramic, Disc: 0.47 µF, 20%, 100 V, Qty. 6, Part No. 8131M100-651-474M, Mfr. Code 72982

   To: C13, Capacitor, Electrolytic Tantalum: 1.0 µF, 20%, 35 V, Qty. 3, Part No. 196D105X0035HE3, Mfr. Code 56289

2. From: C17, Same as C13

   To: C17, Capacitor, Ceramic, Disc: 0.47 µF, 20%, 100 V, Qty. 5, Part No. 8131M100-651-474M, Mfr. Code 72982

3. From: C18, Capacitor, Electrolytic, Tantulum: 1.0 µF, 20%, 35 V, Qty. 2, Part No. 196D105X0035HE3, Mfr. Code 56289

   To: Same as C13

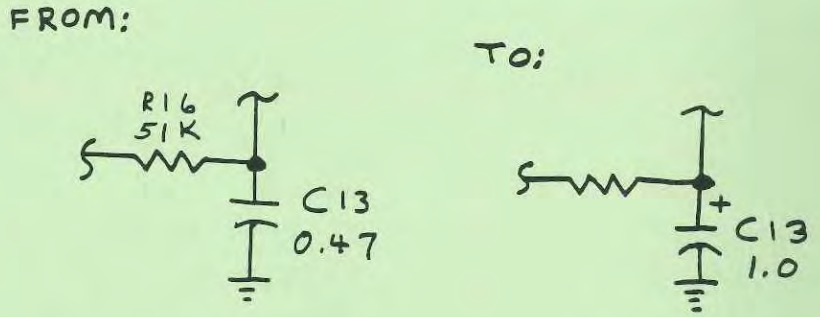
4. From: C19, Same as C18

   To: C19, Same as C13

5. From: C22 Thru C25, Same as C13

   To: C22 Thru C25, Same as C17

1.5.2 Revise Schematic Diagram, Figure 1-23 by changing C13, as shown.



1.6 The resistance value of R37 on the IF Interface (232-A2) has been changed to adjust the real time clock frequency. Change the parts list and schematic diagram as follows.

1.6.1 Revise paragraph 1.10.2, page 1-78 as listed below.

1. From: R37, Resistor, Fixed: 47 kΩ, 5%, 1/4 W, Qty. 1, Part No. RCR07G473JS, Mfr. Code 81349

   To: R37, Same as R1

2. From: R1, Qty. 5

   To: R1, Qty. 6

1.6.2 Revise Figure 1-3 by changing R37 from 47 kΩ to 10 kΩ.

18 November 1983

WJ-8718/232

ADDENDUM IV

The following changes have been incorporated into the RS-232 Option to the WJ-8718 Series Receivers as a PRODUCT IMPROVEMENT.

1. Change Type 796029 Synthesizer Interface to Type 794275-X Synthesizer Interface and Memory. Parts lists and Schematic are included.
2. Change Type 796032 IF Interface to Type 794308-X IF Interface. Parts lists and Schematic are included.

TYPE NUMBER 794275-1 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
*	NOMINAL VALUE, FINAL VALUE FACTORY SELECTED				
BT1	BATTERY NICKEL-CADIUM 2.4V 65MA PC MOUNT	1	418901BD16-1	19209	
CR1	DIODE HI COND HS SW 75PRV SILICON	2	IN4449	80131	
CR2	S/A CR1				
C1	CAP/CER/DISC .1UF 20PCT 100V	7	8131M1C0-651-1C4M	72982	
C2	S/A C1				
C3	S/A C1				
C4	S/A C1				
C5	S/A C1				
C6	CAP/ELEC/TANT 22UF 20PCT 15V	2	196D226X0015KE3	56289	
C7	S/A C6				
C9	CAP/CER/DISC .47UF 20PCT 50V Z5U .300 SQ .200 LEADS	1	34452-1	14632	
C10	CAP/POLY CRBNT 1UF 10PCT 30V	1	ECR105AK	30558	
C11	S/A C1				
C12	S/A C1				

TYPE NUMBER 794275-1 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
C8*	CAP/CER/DISC 680PF 5PCT 100V NPO	1	8121-100-C0G0-681J	72982	
Q1	TRANSISTOR TRANSISTOR	1	2N3251	80131	
R1	NOT USED				
R2	RES/FIXED/FILM 820 OHMS 5PCT .25W	1	CF1/4-820 OHMS/J	09021	
R3	RES/FIXED/FILM 82K 5PCT .25W	2	CF1/4-82K/J	09021	
R4	RES/FIXED/FILM 150 OHMS 5PCT .25W	1	CF1/4-150 OHMS/J	09021	
R5	RES/FIXED/FILM 390 OHMS 5PCT .25W	2	CF1/4-390 OHMS/J	09021	
R6	S/A R3				
R7	RES/FIXED/FILM 10K 5PCT .25W	6	CF1/4-10K/J	09021	
R8	S/A R5				
R9	RES/FIXED/FILM 1.0K 5PCT .25W	5	CF1/4-1K/J	09021	
R10	S/A R9				
R11	S/A R9				
R12	S/A R9				
R13	S/A R9				
R14	RES/FIXED/FILM 3.3K 5PCT .25W	1	CF1/4-3.3K/J	09021	

TYPE NUMBER 794275-1 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
R15	S/A R7				
R16	S/A R7				
R17	S/A R7				
R18	S/A R7				
R19	S/A R7				
U1	INTEGRATED CKT MFP EM E PROM	1	841089 PREL	14632	
U2	NOT USED				
U3	INTEGRATED CKT SOURCE CONTROL DWG FOR HITAGHI 6116-LP3	1	841093	14632	
U4	INTEGRATED CKT ISO-CMOS OCTAL BUS TRANSCEIVER W/3-STATE BUFFERED OP	1	MD74SC245AC	36665	
U5	INTEGRATED CKT ISO-CMOS 3-STATE OCTAL D-TYPE FLIP-FLOP	2	MD74SC374AC	36665	
U6	S/A U5				
U7	INTEGRATED CKT ISO-CMOS OCTAL DECODER/3 BINARY INPUT	2	MD74SC138AC	36665	
U8	S/A U7				
U9	IC PCMOS QUAD 2-INPUT NAND GATE	1	MM74PC00N	27014	

TYPE NUMBER 794275-1 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASS
U10	I C QUAD 2 INPUT AND GATE W/OC OUTPUTS	1	SN74LS09N	01295	
U11	I C	1	SN74LS14N	01295	
U12	I C OCTAL D FLIP FLOP	5	MM74C374N	27014	
U13	S/A U12				
U14	S/A U12				
U15	S/A U12				
U16	S/A U12				
U17	NOT USED				
U18	I C 8 BIT CENTRAL PROCESSING UNIT	1	P8C85A	34649	
VR1	DIODE ZENER 8.2V SILICON	1	IN756A	80131	

TYPE NUMBER 794275-2 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASS
*	NOMINAL VALUE, FINAL VALUE FACTORY SELECTED				
BT1	BATTERY NICKEL-CADIUM 2.4V 65MA PC MOUNT	1	41E901BD16-1	19209	
CR1	DIODE HI COND HS SW 75PRV SILICON	2	1N4449	80131	
CR2	S/A CR1				
C1	CAP/CER/DISC .1UF 20PCT 100V	7	8131M1C0-651-104M	72982	
C2	S/A C1				
C3	S/A C1				
C4	S/A C1				
C5	S/A C1				
C6	CAP/ELEC/TANT 22UF 20PCT 15V	2	196D226X0015KE3	56289	
C7	S/A C6				
C9	CAP/CER/DISC .47UF 20PCT 50V Z5U .300 SQ .200 LEADS	1	34452-1	14632	
C10	CAP/POLY CRBNT 1UF 10PCT 30V	1	ECR105AK	50558	
C11	S/A C1				
C12	S/A C1				

TYPE NUMBER 794275-2 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASS
C8*	CAP/CER/DISC 680PF 5PCT 100V NPO	1	8121-100-C0G0-681J	72982	
Q1	TRANSISTOR TRANSISTOR	1	2N3251	80131	
R1	NOT USED				
R2	RES/FIXED/FILM 820 OHMS 5PCT .25W	1	CF1/4-820 OHMS/J	09021	
R3	RES/FIXED/FILM 82K 5PCT .25W	2	CF1/4-82K/J	09021	
R4	RES/FIXED/FILM 150 OHMS 5PCT .25W	1	CF1/4-150 OHMS/J	09021	
R5	RES/FIXED/FILM 390 OHMS 5PCT .25W	2	CF1/4-390 OHMS/J	09021	
R6	S/A R3				
R7	RES/FIXED/FILM 10K 5PCT .25W	6	CF1/4-10K/J	09021	
R8	S/A R5				
R9	RES/FIXED/FILM 1.0K 5PCT .25W	5	CF1/4-1K/J	09021	
R10	S/A R9				
R11	S/A R9				
R12	S/A R9				
R13	S/A R9				
R14	RES/FIXED/FILM 3.3K 5PCT .25W	1	CF1/4-3.3K/J	09021	

TYPE NUMBER 794275-2 REVISION F SCHEMATIC 570208

TITLE = SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
R15	S/A R7				
R16	S/A R7				
R17	S/A R7				
R18	S/A R7				
R19	S/A R7				
U1	INTEGRATED CKT M232 EM EPROM	1	841087-1 PREL	14632	
U2	NOT USED				
U3	INTEGRATED CKT SOURCE CONTROL DWG FOR HITACHI 6116-LP3	1	841093	14632	
U4	INTEGRATED CKT ISO-CMOS OCTAL BUS TRANSCEIVER W/3-STATE BUFFERED OP	1	MD74SC245AC	36665	
U5	INTEGRATED CKT ISO-CMOS 3-STATE OCTAL D-TYPE FLIP-FLOP	2	MD74SC374AC	36665	
U6	S/A U5				
U7	INTEGRATED CKT ISO-CMOS OCTAL DECODER/3 BINARY INPUT	2	MD74SC138AC	36665	
U8	S/A U7				
U9	IC PCMOS QUAD 2-INPUT NAND GATE	1	MM74PCCON	27014	

TYPE NUMBER 794275-2 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
U10	I C QUAD 2 INPUT AND GATE W/OC OUTPUTS	1	SN74LS09N	01295	
U11	I C	1	SN74LS14N	01295	
U12	I C OCTAL D FLIP FLOP	5	MM74C374N	27014	
U13	S/A U12				
U14	S/A U12				
U15	S/A U12				
U16	S/A U12				
U17	NOT USED				
U18	I C 8 BIT CENTRAL PROCESSING UNIT	1	P8085A	34649	
VR1	DIODE ZENER 8.2V SILICON	1	IN756A	80131	

TYPE NUMBER 794275-3 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
*	NOMINAL VALUE, FINAL VALUE FACTORY SELECTED				
BT1	BATTERY NICKEL-CADIUM 2.4V 65MA PC MOUNT	1	41E9018D16-1	19209	
CR1	DIODE HI COND HS SW 75PRV SILICON	2	1N4449	80131	
CR2	S/A CR1				
C1	CAP/CER/DISC .1UF 20PCT 100V	5	8131M1C0-651-104M	72982	
C2	S/A C1				
C3	S/A C1				
C4	S/A C1				
C5	S/A C1				
C6	CAP/ELEC/TANT 22UF 20PCT 15V	2	196D226X0015KE3	56289	
C7	S/A C6				
C9	CAP/CER/DISC .47UF 20PCT 50V Z5U .300 SQ .200 LEADS	1	34452-1	14632	
C10	CAP/POLY CRBNT 1UF 10PCT 30V	1	ECR105AK	50558	
C11	S/A C1				
C12	S/A C1				

TYPE NUMBER 794275-3 REVISION F SCHEMATIC 570208

TITLE - SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
C8*	CAP/CER/DISC 680PF 5PCT 100V NPO	1	8121-100-C0G0-681J	72982	
Q1	TRANSISTOR TRANSISTOR	1	2N3251	80131	
R1	NOT USED				
R2	RES/FIXED/FILM 820 OHMS 5PCT .25W	1	CF1/4-820 OHMS/J	09021	
R3	RES/FIXED/FILM 82K 5PCT .25W	2	CF1/4-82K/J	09021	
R4	RES/FIXED/FILM 150 OHMS 5PCT .25W	1	CF1/4-150 OHMS/J	09021	
R5	RES/FIXED/FILM 390 OHMS 5PCT .25W	1	CF1/4-390 OHMS/J	09021	
R6	S/A R3				
R7	RES/FIXED/FILM 10K 5PCT .25W	6	CF1/4-10K/J	09021	
R8	S/A R5				
R9	RES/FIXED/FILM 1.0K 5PCT .25W	5	CF1/4-1K/J	09021	
R10	S/A R9				
R11	S/A R9				
R12	S/A R9				
R13	S/A R9				
R14	RES/FIXED/FILM 3.3K 5PCT .25W	1	CF1/4-3.3K/J	09021	

TYPE NUMBER 794275-3 REVISION F SCHEMATIC 570203

TITLE = SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
R15	S/A R7				
R16	S/A R7				
R17	S/A R7				
R18	S/A R7				
R19	S/A R7				
U1	INTEGRATED CKT M488 EM EPROM	1	841C88-1 PREL	14632	
U2	NOT USED				
U3	INTEGRATED CKT SOURCE CONTROL DWG FOR HITACHI 6116-LP3	1	841093	14632	
U4	INTEGRATED CKT ISO-CMOS OCTAL BUS TRANSCEIVER W/3-STATE BUFFERED OP	1	MD74SC245AC	36665	
U5	INTEGRATED CKT ISO-CMOS 3-STATE OCTAL D-TYPE FLIP-FLOP	2	MD74SC374AC	36665	
U6	S/A U5				
U7	INTEGRATED CKT ISO-CMOS OCTAL DECODER/3 BINARY INPUT	2	MD74SC138AC	36665	
U8	S/A U7				
U9	IC PCMOS QUAD 2-INPUT NAND GATE	1	MM74PCCON	27014	

TYPE NUMBER 794275-3 REVISION F SCHEMATIC 570208

TITLE = SYNTHESIZER INTERFACE AND MEMORY PC ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
U10	I C QUAD 2 INPUT AND GATE W/OC OUTPUTS	1	SN74LS09N	01295	
U11	I C	1	SN74LS14N	01295	
U12	I C OCTAL D FLIP FLOP	5	MM74C374N	27014	
U13	S/A U12				
U14	S/A U12				
U15	S/A U12				
U16	S/A U12				
U17	NOT USED				
U18	I C 8 BIT CENTRAL PROCESSING UNIT	1	P8C85A	34649	
VR1	DIODE ZENER 8.2V SILICON	1	IN756A	80131	

TYPE NUMBER 794308-1 REVISION SCHEMATIC 570239

TITLE = IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
CR1	DIODE HI COND HS SW 75PRV SILICON	3	1N4449	80131	
CR2	S/A CR1				
CR3	S/A CR1				
C1	CAP/CER/DISC .1UF 20PCT 50V	9	34475-1	14632	
C2	S/A C1				
C3	S/A C1				
C4	S/A C1				
C5	S/A C1				
C6	CAP/CER/MONO 220PF 5PCT 100V	1	8121-1C0-C0G0-221J	72982	
C7	S/A C1				
C8	CAP/ELEC/TANT 18UF 10PCT 20V	2	196D186X9020KE3	56289	
C9	S/A C8				
C10	S/A C1				
C11	S/A C1				
C12	CAP/ELEC/TANT 22UF 20PCT 15V	1	196D226X0015KE3	56289	
C13	NOT USED				
C14	CAP/ELEC/TANT 4.7UF 20PCT 35V	1	196D475X0035JE3	56289	

TYPE NUMBER 794308-1 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
C15	CAP/ELEC/TANT 47UF 20PCT 20V	1	196D476X0020PE4	56289	
C16	S/A C1				
C17	CAP/CER/DISC .47UF 20PCT 50V Z5U .300 SQ .200 LEADS	1	34452-1	14632	
J1	CONN/RECEP 40 PIN RIGHT ANGLE HEADER ASSY DBL ROW 0.10 CTRS MOD 11	1	1-87567-6	00779	
J2	CONN/RECEP 16 PIN RIGHT ANGLE HEADER ASSY DBL ROW 0.10 CTRS MOD 11	3	87567-4	00779	
J3	S/A J2				
J4	S/A J2				
RN1	RES/NTWK 10 PIN SIP 9 RES 10K 2PCT 0.18W EA 1.60W PKG LOW PROFILE	3	765-1-R10K	73138	
RN2	S/A RN1				
RN3	RES/NTWK 8 PIN SIP 7 RESISTORS 10K 2PCT .18W EA. 1.26W PKG LOW PROFILE	1	764-1-R10K	73138	
RN4	S/A RN1				
R1	RES/FIXED/FILM 10K 5PCT 0.125W	2	CF1/8-10K/J	09021	

TYPE NUMBER 794308-1 REVISION SCHEMATIC 570239

TITLE = IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
R2	RES/FIXED/COMPO 22 OHMS 5PCT .5W	1	RCR20G220JS	81349	
R3	RES/FIXED/COMPO 2.7K 5PCT .5W	1	RCR20G272JS	81349	
R4	S/A R1				
R5	RES/FIXED/FILM 1.0K 5PCT .25W	2	CF1/4-1K/J	09021	
R6	RES/FIXED/FILM 4.7K 5PCT .25W	2	CF1/4 4.7K/J	09021	
R7	RES/FIXED/FILM 20K 5PCT .25W	2	CF1/4-20K/J	09021	
R8	RES/FIXED/FILM 12K 5PCT .25W	2	CF1/4-12K/J	09021	
R9	RES/FIXED/FILM 10K 5PCT .25W	7	CF1/4-10K/J	09021	
R10	S/A R9				
R11	S/A R8				
R12	S/A R7				
R13	S/A R6				
R14	RES/FIXED/FILM 39K 5PCT .25W	1	CF1/4-39K/J	09021	
R15	S/A R9				
R16	RES/FIXED/FILM 82K 5PCT .25W	1	CF1/4-82K/J	09021	
R17	RES/FIXED/FILM 8.2K 5PCT .25W	2	CF1/4-8.2K/J	09021	

TYPE NUMBER 7943C8-1 REVISION SCHEMATIC 570239

TITLE = IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
R18	S/A R9				
R19	S/A R5				
R20	S/A R17				
R21	S/A R9				
R22	RES/FIXED/FILM 750 OHMS 5PCT .25W	1	CF1/4-750 OHMS/J	09021	
R23	S/A R9				
R24	S/A R9				
U1	I C HEX BUFFER 3-STATE	3	MM80C95N	27014	
U2	S/A U1				
U3	INTEGRATED CKT OCTAL BUFFER AND LINE DRIVER/NON-INVERTING OUTPUTS	2	MM74C244N	27014	
U4	I C OCTAL D FLIP FLOP	3	MM74C374N	27014	
U5	S/A U4				
U6	S/A U1				
U7	S/A U3				
U8	INTEGRATED CKT ISO-CMOS 3-STATE OCTAL D-TYPE FLIP-FLOP	1	MD74SC374AC	36665	
U9	S/A U4				

TYPE NUMBER 7943C8-1 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASS'
U10	IC PCMOS QUAD 2-INPUT NAND GATE	1	MM74PC00N	27014	
U11	IC 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER 16 PIN DIP	2	MM74PC138N	27014	
U12	S/A U11				
U13	IC P2CMOS, QUAD 2-INPUT OR GATE	2	MM74PC32N	27014	
U14	IC P2CMOS,HEX INVERTER	1	MM74PC04N	27014	
U15	IC P2CMOS, QUAD 2-INPUT AND GATE	1	MM74PC08N	27014	
U16	I C QUAD BILATERAL SWITCH	1	CD4066BE	02735	
U17	I C QUAD D FLIP FLOP THREE STATE	1	MM74C173N	27014	
U18	I C HEX SCHMITT TRIGGER	1	MM74C14N	27014	
U19	S/A U13				
U20	INTEGRATED CKT ISO-CMOS OCTAL BUS TRANSCEIVER W/3-STATE BUFFERED CP	1	MD74SC245AC	36665	
U21	I C DUAL D FLIP FLOP	1	CD4013BE	02735	

TYPE NUMBER 794308-1 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
U22	I C TRIPLE 2-CHANNEL MULTIPLEXER	1	MC14053BCP	04713	
U23	IC D/A CONN 8-BIT MICROPROCESSOR COMPATIBLE	1	DAC083CLCN	27014	
U24	IC QUAD LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS	1	TLC64CN	01295	
U25	IC A/D CONV 8-BIT W/8 CH ANALOG MUX	1	ADC0808CCN	27014	
VR1	DIODE ZENER 5.1V SILICON	3	1N751A	80131	
VR2	S/A VR1				
VR3	S/A VR1				
XU1	SOCKET/IC 16 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	7	ICN-163-S3-T	06776	
XU2	S/A XU1				
XU3	SOCKET/IC 20 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	8	ICN-203-S3-T	06776	
XU4	S/A XU3				

TYPE NUMBER 7943C8-1 REVISION SCHEMATIC 570239

TITLE = IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
XU5	S/A XU3				
XU6	S/A XU1				
XU7	S/A XU3				
XU8	S/A XU3				
XU9	S/A XU3				
XU10	SOCKET/IC 14 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	9	ICN-143-S3-T	06776	
XU11	S/A XU1				
XU12	S/A XU1				
XU13	S/A XU10				
XU14	S/A XU10				
XU15	S/A XU10				
XU16	S/A XU10				
XU17	S/A XU1				
XU18	S/A XU10				
XU19	S/A XU10				
XU20	S/A XU3				
XU21	S/A XU10				
XU22	S/A XU1				
XU23	S/A XU3				

TYPE NUMBER 794308-1 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
XU24	S/A XU10				
XU25	SOCKET/IC 28 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	1	ICN-286-55-1	06776	

TYPE NUMBER 794308-2 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
CR1	DIODE HI COND HS SW 75PRV SILICON	3	1N4449	80131	
CR2	S/A CR1				
CR3	S/A CR1				
C1	CAP/CER/DISC .1UF 20PCT 50V	9	34475-1	14632	
C2	S/A C1				
C3	S/A C1				
C4	S/A C1				
C5	S/A C1				
C6	CAP/CER/MONO 220PF 5PCT 100V	1	8121-1C0-CCG0-221J	72982	
C7	S/A C1				
C8	CAP/ELEC/TANT 18UF 10PCT 20V	2	196D186X9020KE3	56289	
C9	S/A C8				
C10	S/A C1				
C11	S/A C1				
C12	CAP/ELEC/TANT 22UF 20PCT 15V	1	196D226X0015KE3	56289	
C13	NOT USED				
C14	CAP/ELEC/TANT 4.7UF 20PCT 35V	1	196D475X0035JE3	56289	

TYPE NUMBER 794308-2 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
C15	CAP/ELEC/TANT 47UF 20PCT 20V	1	196D476X0020PE4	56289	
C16	S/A C1				
J1	CONN/RECEP 40 PIN RIGHT ANGLE HEADER ASSY DBL ROW 0.10 CTRS MOD 11	1	1-87567-6	00779	
J2	CONN/RECEP 16 PIN RIGHT ANGLE HEADER ASSY DBL ROW 0.10 CTRS MOD 11	3	87567-4	00779	
J3	S/A J2				
J4	S/A J2				
RN1	RES/NTWK 10 PIN SIP 9 RES 10K 2PCT 0.18W EA 1.60W PKG LOW PROFILE	3	765-1-R10K	73138	
RN2	S/A RN1				
RN3	RES/NTWK 8 PIN SIP 7 RESISTORS 10K 2PCT .18W EA. 1.26W PKG LOW PROFILE	1	764-1-R10K	73138	
RN4	S/A RN1				
R1	RES/FIXED/FILM 12K 5PCT 0.125W	2	CF1/8-12K/J	09021	
R2	RES/FIXED/COMPO 22 OHMS 5PCT .5W	1	RCR20G220JS	81349	
R3	RES/FIXED/COMPO 2.7K 5PCT .5W	1	RCR20G272JS	81349	

TYPE NUMBER 794308-2 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
R4	S/A R1				
R5	RES/FIXED/FILM 1.0K 5PCT .25W	2	CF1/4-1K/J	09021	
R6	RES/FIXED/FILM 4.7K 5PCT .25W	2	CF1/4 4.7K/J	09021	
R7	RES/FIXED/FILM 20K 5PCT .25W	2	CF1/4-20K/J	09021	
R8	RES/FIXED/FILM 12K 5PCT .25W	2	CF1/4-12K/J	09021	
R9	RES/FIXED/FILM 10K 5PCT .25W	1	CF1/4-10K/J	09021	
R10	S/A R9				
R11	S/A R8				
R12	S/A R7				
R13	S/A R6				
R14	RES/FIXED/FILM 39K 5PCT .25W	1	CF1/4-39K/J	09021	
R15	S/A R9				
R16	RES/FIXED/FILM 82K 5PCT .25W	1	CF1/4-82K/J	09021	
R17	RES/FIXED/FILM 8.2K 5PCT .25W	2	CF1/4-8.2K/J	09021	
R18	S/A R9				
R19	S/A R5				
R20	S/A R17				

TYPE NUMBER 7943C8-2 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
R21	S/A R9				
R22	RES/FIXED/FILM 750 OHMS 5PCT .25W	1	CF1/4-750 OHMS/J	09021	
R23	S/A R9				
R24	S/A R9				
U1	NOT USED				
U2	NOT USED				
U3	NOT USED				
U4	NOT USED				
U5	I C OCTAL D FLIP FLOP	2	MM74C374N	27014	
U6	NOT USED				
U7	NOT USED				
U8	INTEGRATED CKT ISO-CMOS 3-STATE OCTAL D-TYPE FLIP-FLOP	1	MD74SC374AC	36665	
U9	S/A U5				
U10	IC PCMOS QUAD 2-INPUT NAND GATE	1	MM74PCCON	27014	
U11	IC 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER 16 PIN DIP	2	MM74PC138N	27014	
U12	S/A U11				

TYPE NUMBER 794308-2 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
U13	IC P2CMOS, QUAD 2-INPUT OR GATE	2	MM74PC32N	27014	
U14	IC P2CMOS,HEX INVERTER	1	MM74PC04N	27014	
U15	IC P2CMOS, QUAD 2-INPUT AND GATE	1	MM74PC08N	27014	
U16	I C QUAD BILATERAL SWITCH	1	CD4066BE	02735	
U17	NOT USED				
U18	I C HEX SCHMITT TRIGGER	1	MM74C14N	27014	
U19	S/A U13				
U20	INTEGRATED CKT ISO-CMOS OCTAL BUS TRANSCEIVER W/3-STATE BUFFERED OP	1	MD74SC245AC	36665	
U21	I C DUAL D FLIP FLOP	1	CD4013BE	02735	
U22	I C TRIPLE 2-CHANNEL MULTIPLEXER	1	MC14053BCP	04713	
U23	IC D/A CONN 8-BIT MICROPROCESSOR COMPATIBLE	1	DAC0830LCN	27014	
U24	IC QUAD LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS	1	TL064CN	01295	

TYPE NUMBER 794308-2 REVISION SCHEMATIC 570239

TITLE - IF INTERFACE PRINTED WIRING ASSY

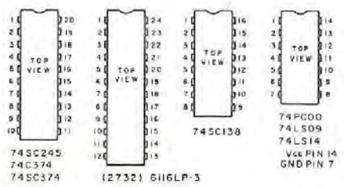
REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASS
U25	IC A/D CONV 8-BIT W/8 CH ANALOG MUX	1	ADC0808CCN	27014	
VR1	DIODE ZENER 5.1V SILICON	3	IN751A	80131	
VR2	S/A VR1				
VR3	S/A VR1				
XU1	SOCKET/IC 16 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	7	ICN-163-S3-T	06776	
XU2	S/A XU1				
XU3	SOCKET/IC 20 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	8	ICN-203-S3-T	06776	
XU4	S/A XU3				
XU5	S/A XU3				
XU6	S/A XU1				
XU7	S/A XU3				
XU8	S/A XU3				
XU9	S/A XU3				
XU10	SOCKET/IC 14 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	9	ICN-143-S3-T	06776	

TYPE NUMBER 794308-2 REVISION SCHEMATIC 570239

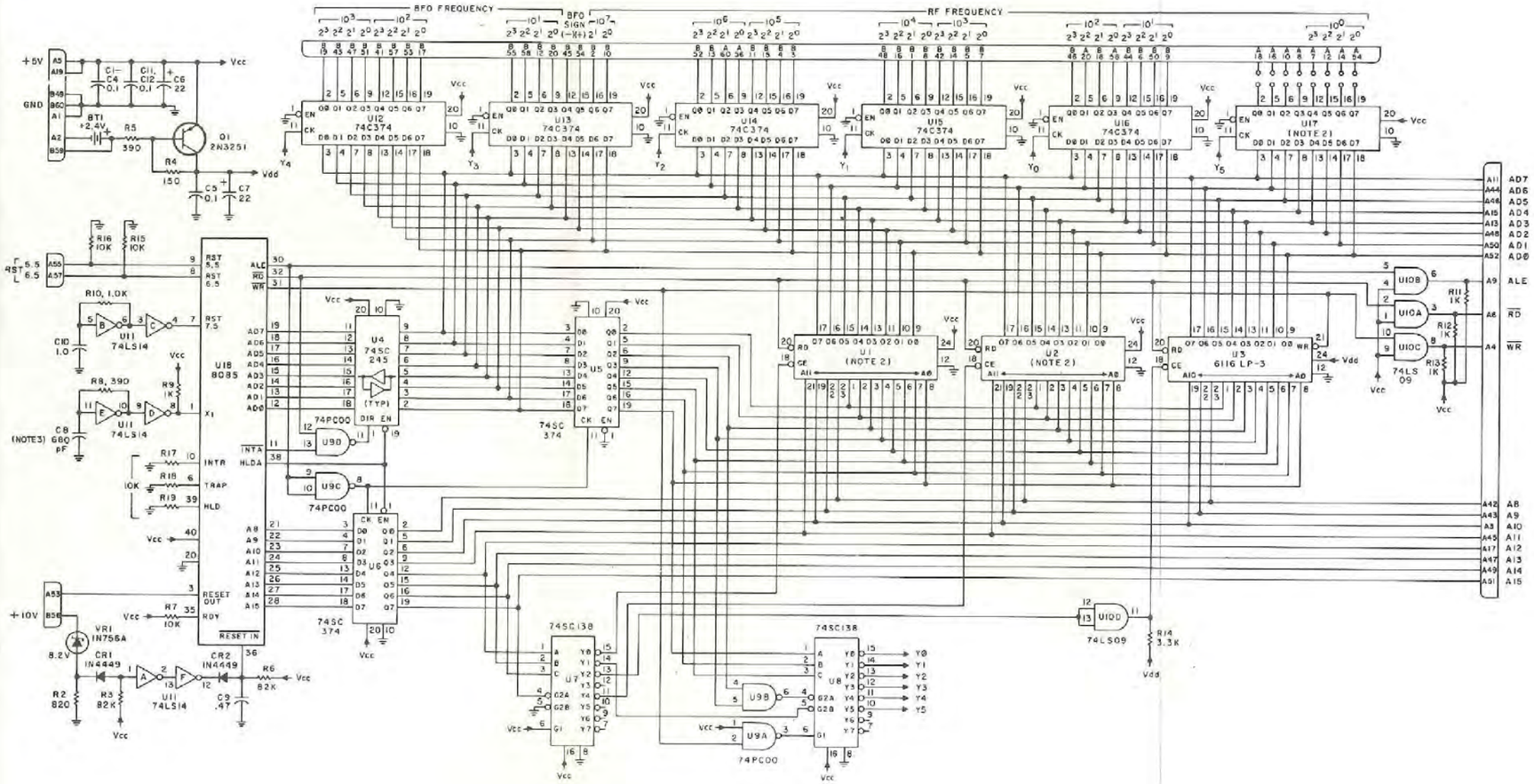
TITLE = IF INTERFACE PRINTED WIRING ASSY

REF DESIG	DESCRIPTION	QTY/ EQPT	PART NUMBER	CODE IDENT	REF ASSY
XU11	S/A XU1				
XU12	S/A XU1				
XU13	S/A XU10				
XU14	S/A XU10				
XU15	S/A XU10				
XU16	S/A XU10				
XU17	S/A XU1				
XU18	S/A XU10				
XU19	S/A XU10				
XU20	S/A XU3				
XU21	S/A XU10				
XU22	S/A XU1				
XU23	S/A XU3				
XU24	S/A XU10				
XU25	SOCKET/IC 28 PIN DIP 0.20 PROFILE W/ANTI-WICKING BARRIER	1	ICN-286-S5-T	06776	

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4 W.
   b) CAPACITANCE IS IN μF.
2. DIFFERENCE BETWEEN TYPE/IC NO.S IS LISTED IN TABLE.
3. NOMINAL VALUE. FINAL VALUE FACTORY SELECTED.



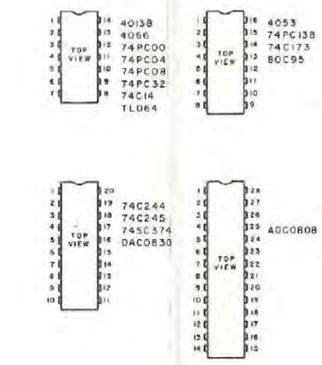
TYPE	U1	U2	U17	OPTION
794275-1	841089	N/U	N/U	8718/MFP
794275-2	841087-1	N/U	N/U	8718/M232
794275-3	841088-1	N/U	N/U	8718/M488-2



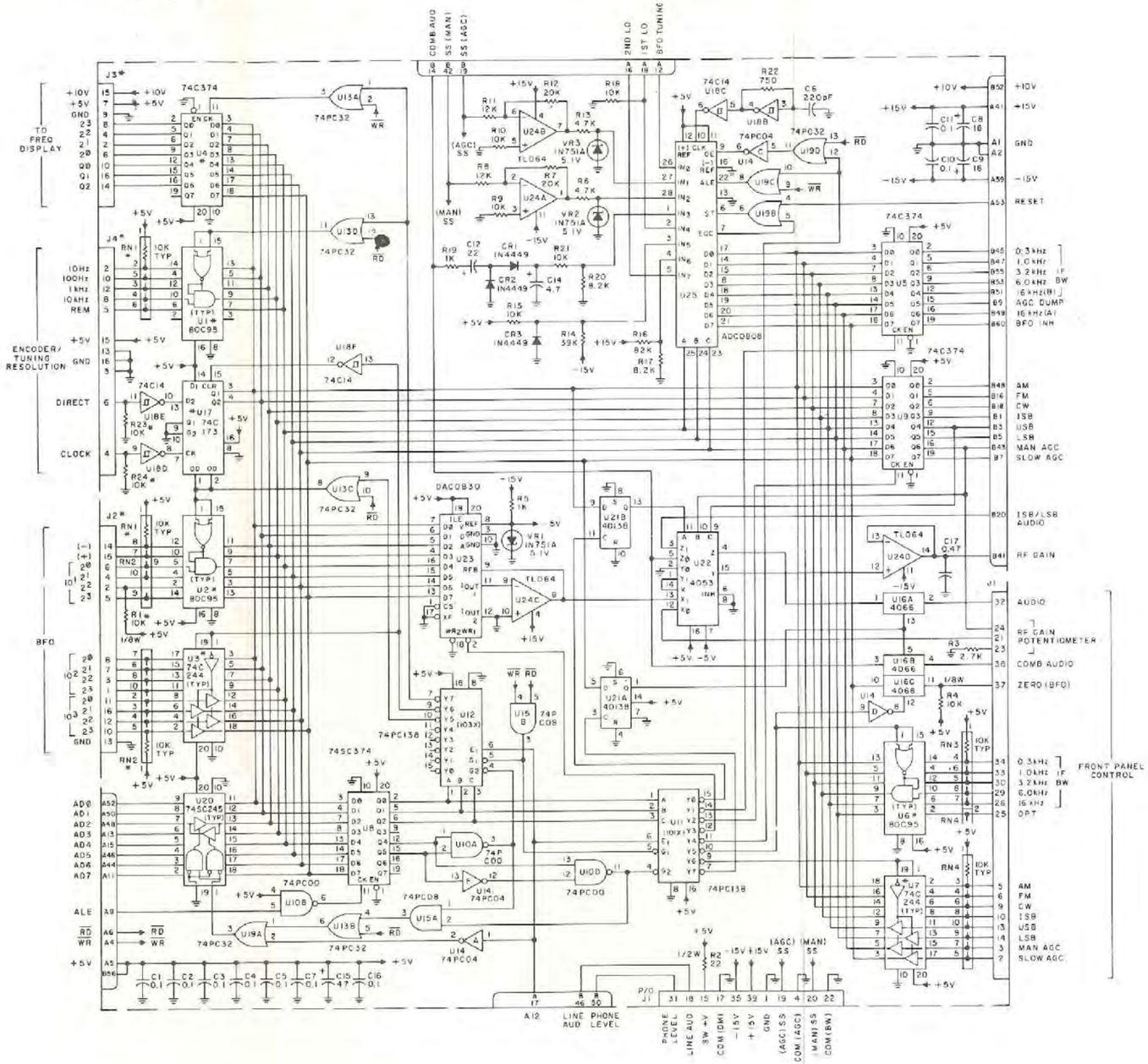
TYPE 794275-X SYNTHESIZER INTERFACE & MEMORY PRINTED CIRCUIT ASSY

11/83

NOTES
1. UNLESS OTHERWISE SPECIFIED,
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN pF.
2. DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE



TYPE	UNIT	COMPONENTS (IN)
794308-1	WJ-8718	AS SHOWN
794308-2	WJ-8718/MFP	OMIT IN FULL



TYPE 794308-X IF INTERFACE PRINTED CIRCUIT ASSY

11/83

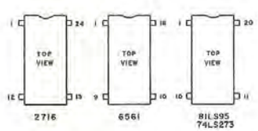
TABLE A

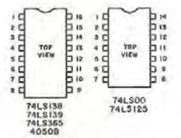
TYPE	U26	U25	U11	U12	USED ON
796029-1	841053	NOT USED	NOT USED	NOT USED	8718/232
796029-2	841036	NOT USED	NOT USED	NOT USED	8718/818
796029-3	841039	NOT USED	NOT USED	NOT USED	8718/488-2
796029-4	841052	NOT USED	NOT USED	NOT USED	8718/232-4
796029-5	841051	NOT USED	NOT USED	NOT USED	8718/232-3
796029-6	841058-1	841058-2	6561	6561	8718/M232
796029-7	841059-1	841059-2	6561	6561	8718/M488-2
796029-8	841057-1	841057-2	6561	6561	8718/MFP

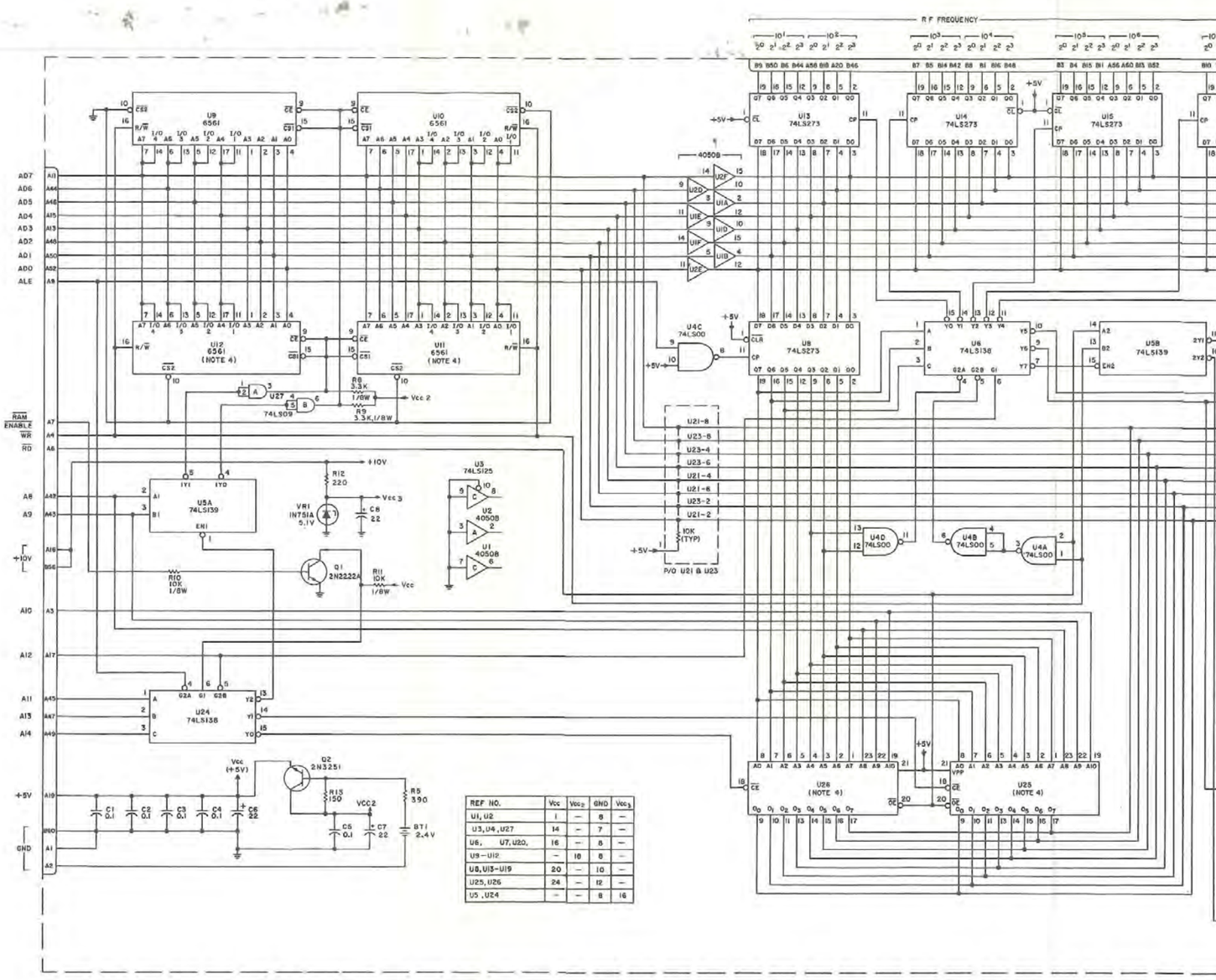
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/4W.
2. FOR VCC & GND SEE TABULATION BLOCK.
3. FOR IC PIN ARRANGEMENT SEE DETAIL "A".
4. DIFFERENCE BETWEEN TYPES IS SHOW IN TABLE "A".

6. "BFO FREQUENCY 10' " WHEN USED IN 8718/232-3 IS NOMENCLATURED AS "RF TUNING 10X"

DETAIL A







REF NO.	Vcc	Vcc_2	GND	Vcc_3
U1, U2	1	—	8	—
U3, U4, U27	14	—	7	—
U6, U7, U20,	16	—	8	—
U9–U12	—	18	8	—
U8, U13–U19	20	—	10	—
U25, U26	24	—	12	—
U5, U24	—	—	8	16

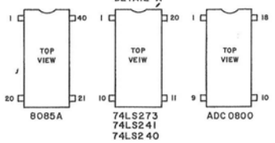
Figure 1-22.(Revised) Type 796029 Synthesizer Interface (232-A1), Schematic Diagram 680014

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b. CAPACITANCE IS IN μF.
2. SEE TABLE I FOR GND & VOLTAGES.
3. SEE DETAIL A & B FOR IC PIN ARRANGEMENTS.
4. DIFFERERENCE BETWEEN TYPES IS SHOWN IN TABLE 2.

TABLE I

REF DESIG	+5V	GND	+15V	−15V	+5 [2]
U1	40	20			
U9,10,11,12,13,14,	20	10			
U20	10	18			
U7,8	16	8			
U2, 5, 21	14	7			
U22		8			8
U15	1	8			
U17, 18			9,13	4	
U19	13	2			
U4		7			14
U3		7			14

DETAIL A



DETAIL B

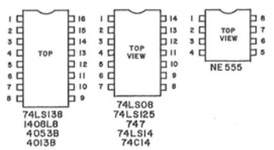


TABLE 2

TYPE	W1	R19
796032-1	NOT USED	AS SHOWN
796032-2	AS SHOWN	NOT USED

Figure 1-43. Type 796032-2 IF Interface (MFP-A3), Schematic Diagram 680016

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1.1 GENERAL DESCRIPTION

The WJ-8718/232 Option, when installed in the WJ-8718 HF Receiver, permits integration of the receiver with remote control equipment that is compatible with the EIA Standard RS-232-C format. Up to 32 WJ-8718 HF Receivers, equipped with the option, can be addressed to receive or transmit (Listen/Talk) by one controller via the RS-232-C bus.

The receiver control block is built around a microprocessor. Inputs to the control block consist of encoded data which come from the receiver's front panel controls or from an external control device via the receiver's rear panel I/O port. The receiver's control block processes the encoded inputs and develops data which are used to drive the synthesizer, IF, gain mode, and demodulator circuits in the receiver.

The WJ-8718/232 Asynchronous I/O Board handles communications between the receiver's control block and the remote control device. The functions of the I/O board include data transfer, handshake protocol, receiver addressing, and interrupt requests. Alternate connections on the I/O Board allow the WJ-8718/232 Option to be converted to comply with MIL. STD. 188C. A switch assembly on the I/O Board permits binary-coded selection of baud rates for asynchronous transmit and receive operation. An external baud rate, established by the remote control device, can be incorporated through alternate connections on the I/O Board.

Receiver parameters that can be controlled and monitored are tuned and BFO frequencies, detection mode, gain mode, and IF bandwidth. RF gain can be controlled in the receiver manual gain mode via remote control in a command sequence. Signal strength is monitored when the receiver is requested to transmit.

1.2 MECHANICAL DESCRIPTION

The WJ-8718/232 Option for the WJ-8718 HF Receiver consists of three printed circuit boards mounted by edge connectors to the receiver's I/O Motherboard, A6. The 232-A1 board replaces the receiver's Manual Tuning Up/Down Counter Board, A6A1; the 232-A2 board replaces the receiver's Front Panel Interconnect Board, A6A2. Multiconductor cables provide the interboard wiring and connections to two 25-pin D-series connectors mounted on the receiver rear panel.

Cabling from the receiver to remote control equipment should conform to EIA Standard RS-232-C.

1.2.1 EQUIPMENT SUPPLIED

The WJ-8718/232 Option consists of three printed circuit boards: Type 796029, Synthesizer Interface Board (232-A1); Type 796032, IF Interface Board (232-A2); and Type 796037, Asynchronous I/O Board (232-A3). Interconnect cables (W1, W2, and W3) and the following installation hardware items are also supplied: 2 adapter plates, 8 Phillips head screws, 8 lockwashers, and 4 hex nuts.

1.2.2 EQUIPMENT REQUIRED BUT NOT SUPPLIED

To install the WJ-8718/232 Option, the technician will require the following: AWG #30 wire-wrap wire, a 1.5-inch by 0.2-inch by 0.01-inch copper conductor strip, and 1.5-inch wide plater's tape.

To connect additional receivers in a "daisy-chained" configuration (Figure 1-3), flat 25-wire cable must be used. The cable should be connected as shown in Figure 1-3; recommended connectors are listed in Table 1-1.

Table 1-1. Recommended Receiver-To-Receiver Connectors

Quantity	Item	Part Number	Recom. Vendor
4	Male Screw Retainer Kit	205980-1	00779
1	Connector, Receptacle	206653-1	00779
1	Connector, Plug	206646-1	00779

To control and monitor the WJ-8718/232 Option equipped receiver, a remote control unit compatible with the EIA RS-232-C Interface is required.

1.3 INSTALLATION PROCEDURES

The following procedures outline the WJ-8718 HF Receiver modifications and the WJ-8718/232 assembly and mounting instructions. Figure 1-1, the WJ-8718/232 Installation Diagram, should be referred to as necessary.

1.3.1 REMOVING TYPES 791828 AND 791575 BOARDS FROM RECEIVER

1. Remove power from the receiver.

2. Loosen the 34 quarter-turn fasteners securing the receiver top cover and lift the cover from the receiver.

3. In the receiver, locate the Type 791828, Front Panel Interconnect Assembly, A6A2.

4. Loosen the A6A2 board and lift it to the top of the receiver. Remove cable connector A10P1 from right-angle board connector, J1. Remove the A6A2 board from the receiver.

5. In the receiver, locate the Type 791575-1 or 791575-2, Manual Tuning Up/Down Counter Assembly, A6A1. If the assembly is Type 791575-2, perform steps 6 and 7 of the following procedure; if the assembly is Type 791575-1, omit step 6 and perform step 7 only.

6. Remove cable connector A6A1J1 from the rear panel location marked REMOTE INPUT, by removing the two nuts, lockwashers, flatwashers, and screws that secure the A6A1J1 connector.

7. Loosen the A6A1 board and lift it to the top of the receiver. Remove cable connector A8P1 from J2, A9P1 from J3, and A7A1P1 from J4. Remove the board from the receiver.

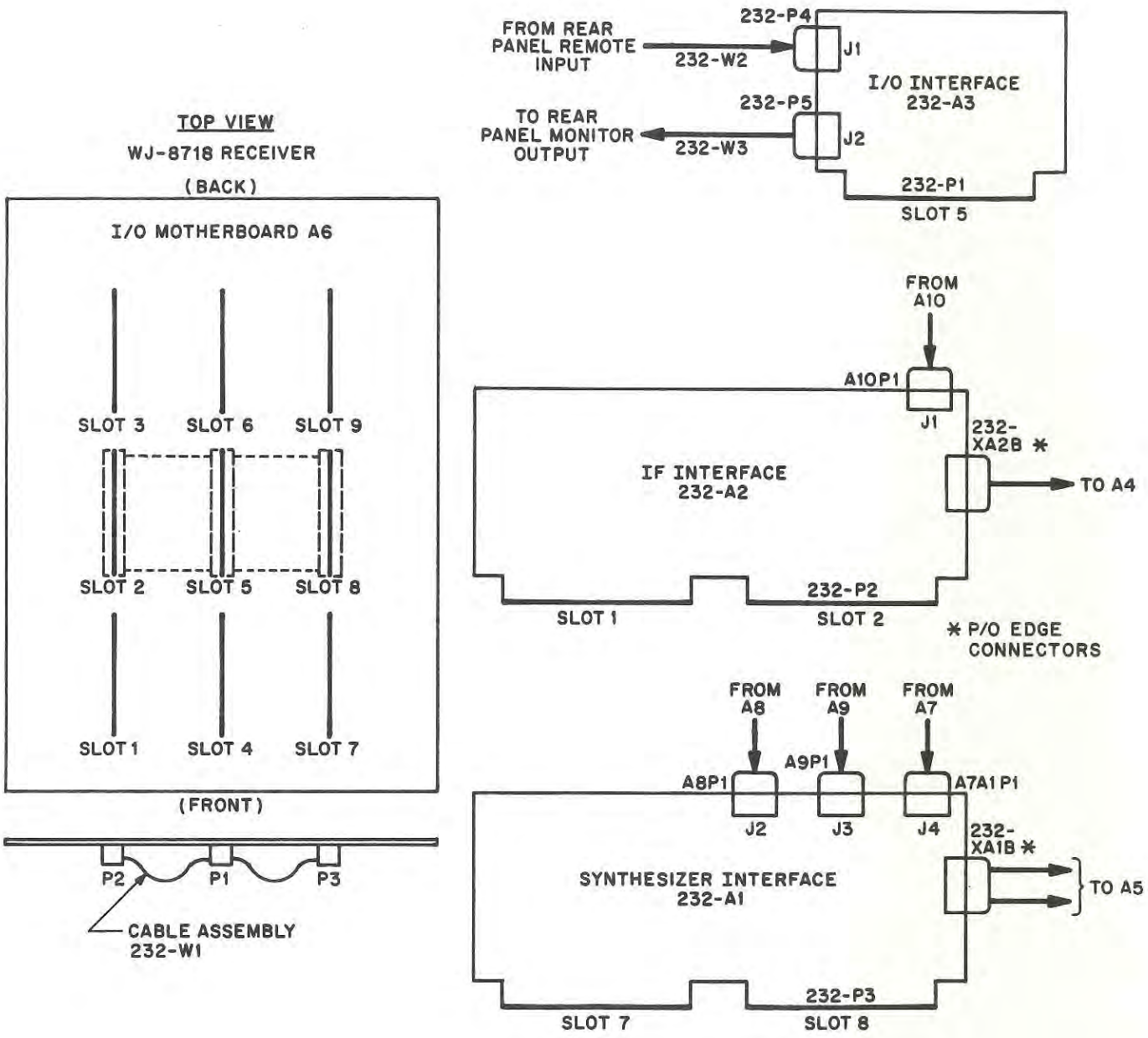

Figure 1-1. Installation Diagram

1.3.2 MODIFICATION OF TUNING RESOLUTION BOARD

Proceed to execute the instructions outlined in this paragraph if the receiver contains Type 791575-1 or 791575-2 Manual Tuning Modules. If the receiver contains a Remote Control Module, disregard the remainder of paragraph 1.3.2 and proceed to paragraph 1.3.3.

1. Locate the Type 791575-1 or 791575-2 Manual Tuning Module, A7, in the receiver.

2. Locate the Type 791589, Tuning Resolution Board, A7A1, on the Tuning Module and note the revision code of the printed circuit board. The revision code is an alphabetical, upper-case letter enclosed in a circle, and is etched on the lower section of the board.

3. If the revision code is letter D or a letter that alphabetically follows D, proceed to paragraph 1.3.3; if the revision code is letter B or C, the A7A1 board must be modified using the following procedure.

4. Carefully, so that the A7A1P1 cable previously removed from A6A1 is not damaged, remove the Type 791575-1 or 791575-2 Manual Tuning Module, A7, from the receiver front panel by removing the four securing screws. Retain the screws, lockwashers, and flatwashers for the re-assembly effort.

5. Position the A7 module with the back (side opposite switch) of A7A1 accessible for modification. Refer to Figure 1-2, and proceed to modify the Tuning Resolution Board as follows.

6. On the left side of the board, immediately below the pad labeled C, cut the track in two places, 1/32-inch (minimum) apart. Strip the track between the cuts and tin the edges of the bare copper.

7. On the left side of the board, immediately to the left of the pad labeled E1, cut the track in two places, 1/32-inch (minimum) apart. Strip the track between the cuts and tin the edges of the bare copper.

8. Refer to Figure 1-2 and note the location of Jumper Wire #1. Determine the distance to be spanned by the wire; cut a length of AWG #30 wire-wrap wire as required and strip the ends. Wrap and solder one end of the wire to the paddle board terminal at pad E1. Lay the opposite end of the wire on the track previously separated from pad C and solder the wire to the track.

9. On the right side of the board, between pads E13 and E15, cut the track in two places 1/32-inch (minimum) apart. Strip the track between the cuts and tin the edges of the bare copper.

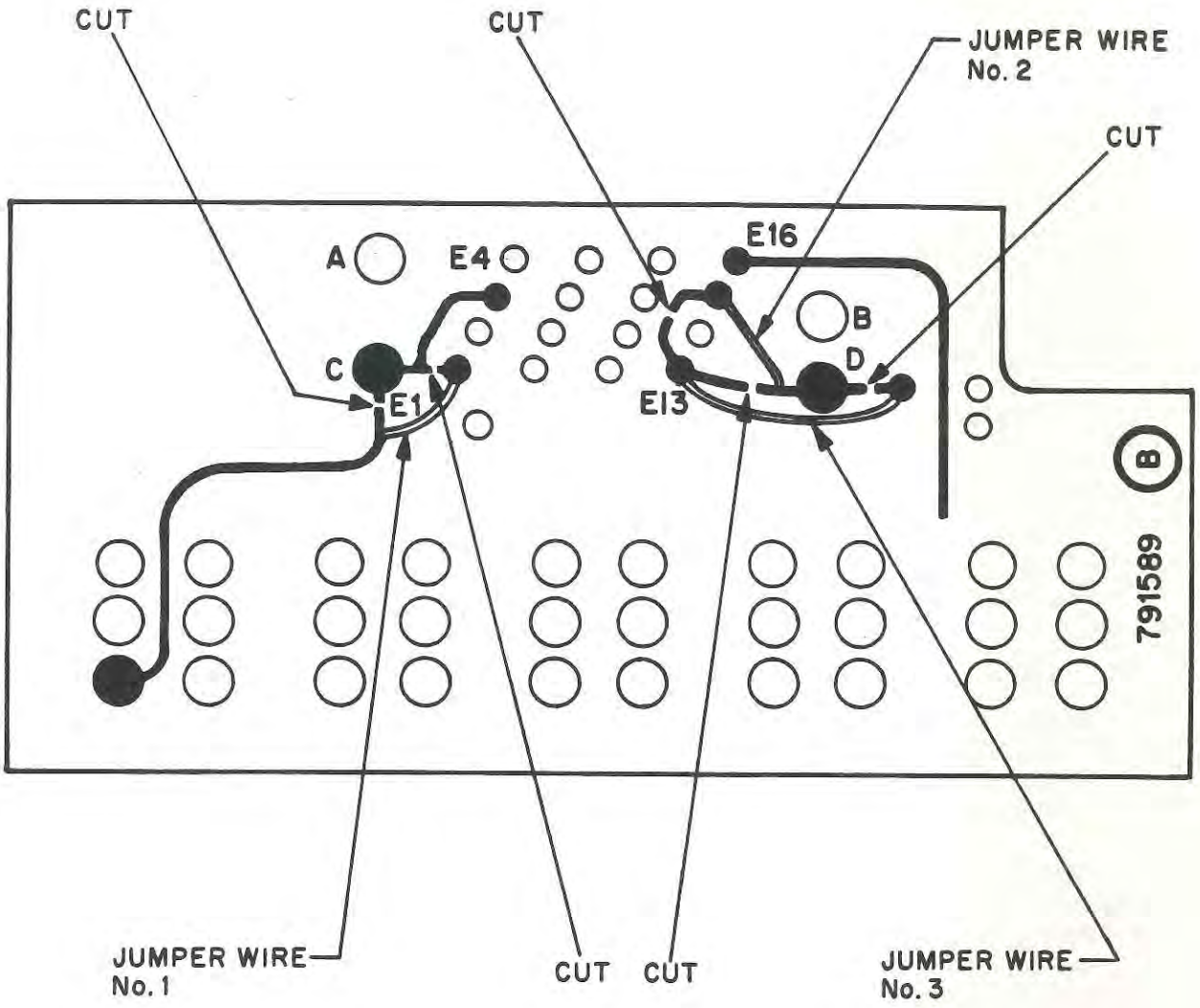

Figure 1-2. Tuning Resolution Board Modifications

10. On the right side of the board, between pad E13 and pad D, cut the track in two places, 1/32-inch (minimum) apart. Strip the track between the cuts and tin the edges of the bare copper.

11. On the right side of the board, to the right of pad D, cut the track in two places, 1/32-inch (minimum) apart. Strip the track between the cuts and tin the edges of the bare copper. Remove the solder from the feed-through hole to the right of the cuts.

12. Refer to Figure 1-2 and note the locations of Jumper Wires #2 and 3. Determine the length of wire required and cut two pieces of AWG #30 wire-wrap wire. Strip both ends of the wires.

13. Wrap and solder one end of Jumper Wire #2 to the paddle board terminal at pad E15. Lay the opposite end of the wire on the track to the left of pad D and solder the wire to the track.

14. Wrap and solder one end of Jumper Wire #3 to the paddle board terminal at pad E13. Place the opposite end of the wire through the feed-through hole to the right of pad D and solder. Trim and tin the end of the wire extending through the opposite side of the board.

15. Clean the board with flurocarbon or hydrocarbon solvent.

CAUTION

Do not allow the solvent into the switch mechanism. The solvent will remove the switch lubricant and adversely affect the operation of the switch.

16. Replace the Manual Tuning Module in the front panel and secure with the screws and washers removed in step 4, above.

1.3.3 MODIFICATION OF IF MOTHERBOARD

Loosen the 34 quarter-turn fasteners from the receiver's bottom cover and remove the cover. Locate the Type 791569 IF Motherboard, A4, in the receiver, and note the revision code. The code is an upper-case letter enclosed in a circle and etched on the lower side of the board. If the A4 board is revision E, proceed to paragraph 1.3.4; if the revision code letter alphabetically precedes the letter E, modify the A4 board as follows:

1. Locate the A4 connector XA2; on XA2 locate pins 59 and 60.

2. Place a copper conductor bus strip (1.5- by 0.2- by 0.10-inches in size) over the ground plane at XA1 terminals 59 and 60; center the strip evenly on ground planes at XA1 and XA2. The bus strip should be insulated with plater's mylar tape where it passes over the board circuitry.

3. Sweat-solder the bus strip to the ground plane at XA2 terminals 59 and 60 and to the ground plane at XA1 near terminals 59 and 60.

4. Clean all solder joints with flurocarbon or hydrocarbon solvent.

1.3.4 MOUNTING THE WJ-8718/232 COMPONENTS

1. Position the receiver, bottom side up, and connect the 232-W1 ribbon cable assembly (part number 280097) over slots 2, 5, and

8 in the I/O Motherboard, A6, as shown in Figure 1-1. Seat the connectors securely.

2. Turn the receiver right side up.

3. Position the two adapter plates (part number 180027-1) on the inside of the receiver rear panel at the locations labeled REMOTE INPUT and MONITOR OUTPUT. Secure the plates to the rear panel using two Phillips-head screws (part number S260047) and two lockwashers (part number S140257) for each plate.

4. Secure connector 232-J1 on the 232-W2 cable assembly (part number 380059) to the adapter plate at the rear panel REMOTE INPUT using two Phillips-head screws (part number S260047), two lockwashers (part number S140257), and two hex nuts (part number S260125).

5. Using the remaining two screws, lockwashers, and nuts described in step 4 above, secure connector 232-J1 on the 232-W3 cable assembly (part number 380060-1) to the adapter plate at the rear panel MONITOR OUTPUT.

6. Position the Type 796029 Synthesizer Interface Assembly (232-A1) near slots 7 and 8 of the I/O Motherboard, A6. Locate the A7A1P1 cable from the Tuning Resolution Board and install the cable in 232-A1 board connector J4, identified by brown color marker.

7. Locate the A9P1 cable from the BFO Switch and install the cable in 232-A1 board connector J3, identified by orange color marker.

8. Locate the A8P1 cable from the Frequency Display Board and install the cable in 232-A1 board connector J2, identified by red color marker.

9. Dress the cables, position the 232-A1 board in the I/O Motherboard slot connectors 7 and 8, and seat securely.

10. Position the Type 796037 Asynchronous I/O Assembly (232-A3) near slot 5 of the I/O Motherboard.

11. Locate cable assembly 232-W2, installed at the rear panel REMOTE INPUT, and install connector 232-P4 in 232-A3 board connector J1.

12. Locate cable assembly 232-W3, installed at the rear panel MONITOR OUTPUT, and install connector 232-P5 in 232-A3 board connector J2.

13. Dress the cables, position the 232-A3 board in slot connector 5 in the I/O Motherboard, and seat securely.

14. Position the Type 796032 IF Interface Assembly (232-A2) near slots 1 and 2 of the I/O Motherboard. Locate the A10P1 cable from the Lower Panel Control and install the cable in 232-A2 board connector J1.

15. Dress the cable, position the 232-A2 board in I/O Motherboard slots 1 and 2, and seat securely.

16. Replace receiver top and bottom covers.

1.4 PREPARATION FOR OPERATION

Prior to remote operation of a WJ-8718/232 Option equipped receiver, the receiver must be placed in the remote operating mode and remote operating parameters must be established on the I/O board switches and connections, as described in the paragraphs that follow. Refer to Figure 1-24, the Asynchronous I/O Board Schematic Diagram, to correlate the descriptions.

1.4.1 REMOTE OPERATING MODE

A receiver to be addressed as a listener must be placed in the remote operating mode by depressing the front panel TUNING DISABLE button. The receiver can be addressed to talk regardless of the TUNING DISABLE switch position. Local or remote operating mode cannot be established by remote command.

1.4.2 BAUD RATE

Baud rate is established by precoded entries to the S1 switch assembly on the Asynchronous I/O Board. An open switch denotes binary 1 and a closed switch denotes binary 0. Table 1-2 lists the baud rate codes. Prior to shipment, the switches are set for a baud rate of 1200.

Table 1-2. Baud Rate Codes

Baud Rate	S1-1	S1-2	S1-3	S1-4
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
134.5	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2000	1	0	0	1
2400	1	0	1	0
3600	1	0	1	1
4800	1	1	0	0
7200	1	1	0	1
9600	1	1	1	0
19200	1	1	1	1

1.4.3 SYNCHRONOUS OPERATION

The WJ-8718/232 Option is normally wired for asynchronous operation. Alternate connections on the I/O board at P3 and P4 (Figure 1-24) allow application of synchronous receive and transmit timing signals from the remote control equipment; however, if synchronous operation is desired, the program memory devices must be returned to Watkins-Johnson for re-programming.

1.4.4 RECEIVER ADDRESS AND PARITY CHECK

Up to 32 properly addressed receivers can be controlled by one remote device. As shown in Figure 1-3, the receivers are series-connected, or "daisy-chained", and only one receiver is interfaced directly to the remote control equipment. The serial data stream from the remote control equipment is actively repeated to all receivers in the chain, but only the addressed receiver "recognizes" its address and accepts the data.

Receiver address is established by five switch settings in the S2 switch assembly on the I/O board. Table 1-3 lists the functions of the switch assembly. A closed switch denotes a binary 1 and an open switch denotes a binary 0. Valid receiver addresses are binary coded from 0 through 31, as listed in Table 1-4.

Table 1-3. Switch Assembly (S2) Functions

S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
Master/Slave	Parity Enable	Parity Bit	2^4	2^3	2^2	2^1	2^0
			Receiver Address				

Switch S2-8 is opened (0) if the receiver is to be a slave; as a slave the receiver can be commanded and monitored by a remote control device. Switch S2-8 is closed (1) if the receiver is to be a master. Configured as a master, the receiver will constantly transmit parameter data, allowing master-slaving of two receivers.

Switches S2-6 and S2-7 are used if the remote control equipment provides a parity bit. If S2-7 is closed, a parity bit is expected and must be sent with the remote transmission; if S2-7 is open, a parity bit cannot be sent. S2-6 is closed (1) if even parity is desired and opened (0) if odd parity is desired.

Table 1-4. Receiver Address Codes

Receiver Address	S2-5	S2-4	S2-3	S2-2	S2-1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1

Table 1-4. Receiver Address Codes (Concluded)

Receiver Address	S2-5	S2-4	S2-3	S2-2	S2-1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0
31	1	1	1	1	1

NOTE: 0 = open, 1 = closed

1.4.5 MIL-188C

Alternate connections on the Asynchronous I/O Board at J4, J8, and J19 allow the option to function at Military Standard 188C levels. See the Asynchronous I/O Board Schematic Diagram, Figure 1-24, for connection details.

1.5 OPERATION

1.5.1 RS-232-C INTERFACE BUS

A receiver equipped with the WJ-8718/232 Option is ready to be interfaced with a remote control device compatible with the RS-232-C EIA Standard Interface Bus. The option utilizes 10 of the 25 available interchange channels provided by the bus: two for ground, two for data transfer, two for optional synchronous timing inputs, and four for handshake protocol. The interface point between receiver and remote control equipment is the 25-pin, D-series connector at the REMOTE INPUT port on the receiver rear panel. A 25-pin connector at the receiver's rear panel MONITOR OUTPUT port is the interface point for connecting the next receiver in the series chain. Up to 32 WJ-8718 HF Receivers equipped with the WJ-8718/232 Option can be controlled by one remote control device, as shown in Figure 1-3.

Table 1-5 lists the RS-232-C connection pin numbers with the respective interchange signals and functions.

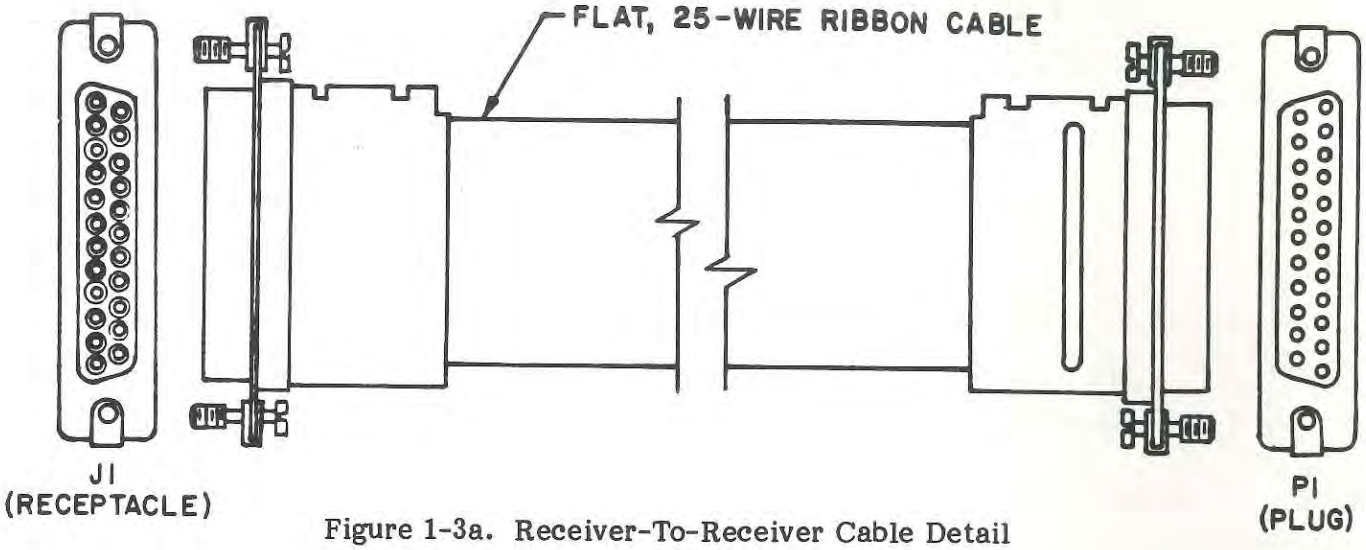

Figure 1-3a. Receiver-To-Receiver Cable Detail

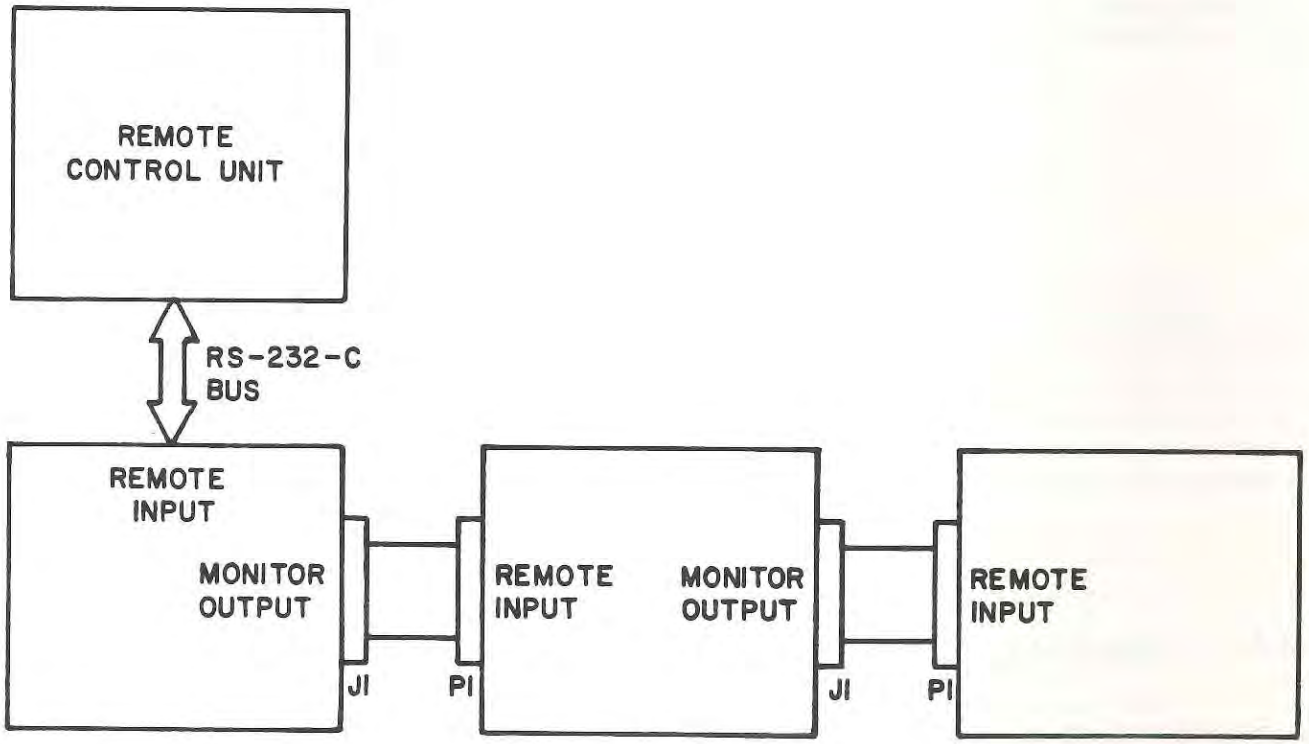

Figure 1-3b. "Daisy-Chained" Configuration

Figure 1-3. Equipment Connections

Table 1-5. RS-232-C Connector Pin Assignments

Pin Number	Signal	Description
1	P-GND	Protective Ground
2	TxD	Transmitted Data
3	RxD	Received Data
4	RTS	Request to Send
5	CTS	Clear to Send
6	DSR	Data Set Ready
7	S-GND	Signal Ground
15	SYNC - TxC	Transmit Timing Signal
17	SYNC - RxC	Receive Timing Signal
20	DTR	Data Terminal Ready

1.5.2 CONTROL AND MONITOR DATA FORMAT

1.5.2.1 Byte Structure

The I/O software structure of the WJ-8718/232 Option consists of a series of 11-bit binary coded words (if parity is used), presented in a pre-determined sequence. Each byte is composed of a start bit, eight data bits, a parity bit (if parity is enabled), and a stop bit. Figure 1-4 illustrates the byte structure. Binary coded logic levels are high (-6 V) or low (+6 V).

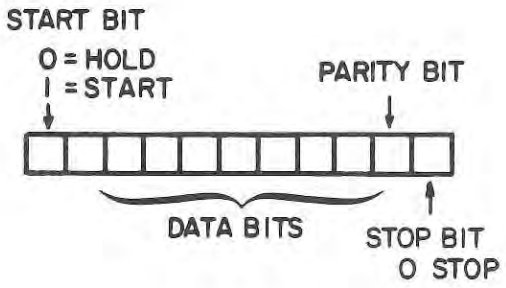

Figure 1-4. Byte Structure

1.5.2.2 Data Format: Tier 1

Full status parameter data of a standard WJ-8718 HF Receiver equipped with the WJ-8718/232 Option is contained in seven bytes; these seven bytes, plus address and data definition bytes and a byte for Tier 2 access, comprise Tier 1 of the I/O software structure. Tier 2 is discussed in paragraph 1.5.2.6. Tier 1 is structured as follows:

1. Byte 1: Receiver Address Byte.
2. Byte 2: Data Information Definition Byte (DID).

3. Bytes 3 through 9 (10): In monitor mode, Byte 3 is the address byte returned from the receiver to controller and Bytes 4 through 10 are data. In command mode, Bytes 3 through 9 are parameter data (controller to receiver).

4. Byte 10 or 11: Tier 2 Access Byte.

1.5.2.3 Receiver Address Byte

The data bits in the first byte (controller to receiver) determine which receiver is to be referenced. Up to 32 receivers can be controlled and monitored by one controller (such as the WJ-9644A Asynchronous Controller) via the WJ-8718/232 Option. As shown in Table 1-6, five bits of the receiver address byte allow for 32 unique binary-coded addresses from 0 through 31 (Table 1-4). The three most significant bits of the address are a binary code (110) that uniquely identifies the function (receiver address) of the byte.

In the monitor mode, the receiver address byte is returned to the controller by the receiver prior to the transmission of data (receiver to controller).

Table 1-6. Receiver Address Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	0					
Address Byte Code			Receiver Address: Range 0 0 0 0 0 - 1 1 1 1 1				

1.5.2.4 Data Information Definition (DID) Byte

Byte 2 is the Data Information Definition (DID) Byte, as shown in Table 1-7. The three most significant bits of the DID byte are a binary code (111) which uniquely defines Byte 2 as a DID byte. The 2 bit of the DID byte is the command/monitor bit, which defines the function of the data bytes to follow Byte 2. If the 2^4 bit is logic 1, the controller desires to command the receiver and will transmit receiver parameter data in the byte or bytes to follow Byte 2. If the 2^4 bit is logic 0, the controller desires to monitor the receiver; the receiver will transmit the address byte (paragraph 1.5.2.3), and the byte or bytes that follow will contain the current status of the addressed receiver (transmitted by the receiver).

Table 1-7. DID Byte

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	1	1					
DID Byte Code			C/M	S/A	Register: 0 0 0 - 1 1 0		

C/M = Command (1) or Monitor (0)
S/A = Single (1) or All (0) Bytes

The 2^3 bit of the DID defines the number of data bytes to succeed Byte 2; a logic 1 indicates a single byte and a logic 0 indicates all bytes.

Table 1-8. Register Parameter Data

BYTE		ADDRESS			DATA WORD							
MON	COM	R1	R2	R3	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
4	3	0	0	0	2^3 2^2 2^1 2^0 10^1 BFO FREQ				R/L	+/- BFO	2^1 2^0 10^7 TUNED FREQ	
5	4	0	0	1	2^3 2^2 2^1 2^0 10^6 TUNED FREQ				2^3 2^2 2^1 2^0 10^5 TUNED FREQ			
6	5	0	1	0	2^3 2^2 2^1 2^0 10^4 TUNED FREQ				2^3 2^2 2^1 2^0 10^3 TUNED FREQ			
7	6	0	1	1	2^3 2^2 2^1 2^0 10^2 TUNED FREQ				2^3 2^2 2^1 2^0 10^1 TUNED FREQ			
8	7	1	0	0	B1 B2 B3 BANDWIDTH			G1 G2 GAIN MODE		D1 D2 D3 DETECTION MODE		
9	8	1	0	1	2^3 2^2 2^1 2^0 10^3 BFO FREQ				2^3 2^2 2^1 2^0 10^2 BFO FREQ			
10	9	1	1	0	0 *	X NOT USED		R5 R4 R3 R2 R1 R0 MONITOR = SIGNAL STRENGTH COMMAND = RF GAIN				

* COMMAND: AGC DUMP, MONITOR: FAULT (for future expansion)
NOTE: BFO and TUNED frequencies in BCD (Hz)

Function Codes

R/L: 1 = Remote, 0 = Local

+/- BFO: 1 = +; 0 = -

Bandwidth (in kHz)	B1	B2	B3
16	0	0	0
6	0	0	1
3.2	0	1	0
1.0	0	1	1
0.3	1	1	0
OPT	1	0	1

Gain Mode	G1	G2
FAST AGC	0	0
MANUAL	0	1
SLOW AGC	1	0

Detection Mode	D1	D2	D3
AM	0	0	0
FM	0	0	1
CW	0	1	0
USB	0	1	1
LSB	1	1	0
ISB	1	0	1

RF Gain (Command)	R5	R4	R3	R2	R1	R0	Signal Strength (Monitor)
Maximum Gain	0	0	0	0	0	0	No Signal
Minimum Gain	1	1	1	1	1	1	Maximum Signal

The remaining three bits of the DID byte contain a binary coded register address. All receiver parameters are stored in seven 8-bit registers, addressed in binary code from 0 through 7. If all parameter data are to be transmitted, the logic levels of the three register address bits are irrelevant; however, if one word of receiver parameter data is to be transmitted, the 3-bit binary code for the desired register must be established in the 2^0, 2^1, and 2^2 bits of the DID byte (paragraph 1.5.2.5).

1.5.2.5 Data Bytes

If all receiver parameters are to be controlled, the bytes following the DID Byte will contain data transmitted from receiver to controller or from controller to receiver, as listed in Table 1-8 (see preceding page). If all receiver parameters are to be monitored, Byte 3 will be the address return byte followed by data, Bytes 4 through 10. Transmission of less than complete parameter data requires that the register associated with a particular byte of data be addressed in the DID byte. The selected data will then be transmitted as Byte 3 or 4. Paragraph 1.5.2.7 contains examples of data formats for full and partial status transmissions, in monitor and command modes.

1.5.2.6 Tier 2 Access Byte

A second tier containing four pages of eight bytes each is available and is accessed by the byte shown in Table 1-9. The 3 most significant bits of the byte are the DID code (111), the 2^4 and 2^3 bits are a page code, and the remaining three bits are the address code for the second tier.

Table 1-9. Tier 2 Access Byte

2^7	2^6	2^5	2^4 2^3	2^2	2^1	2^0
1	1	1		1	1	1
DID CODE			PAGE CODE	TIER 2 CODE		

Page Code

Page	2^4	2^3
1	0	0
2	0	1
3	1	0
4	1	1

1.5.2.6.1 Tier 2

Tier 2 contains four pages of eight bytes each. At this point in time, the four most significant bits of the 000 register byte on page 1 are the only bits of Tier 2 with an assigned function. These four bits contain the 10^0 digit (in BCD form) of tuned frequency if the WJ-8718 HF Receiver is equipped with both the WJ-8718/232 and WJ-8718/1 Hz Options. The remaining bytes in Tier 2 are available for future expansion. Table 1-10 is the data format for Byte 1 on Page 1 of Tier 2. This byte must be preceded by a receiver address byte, a Tier 2 access byte, and a DID byte containing the register address 000. See paragraph 1.5.2.7 for an example of data format requiring access to Tier 2.

Table 1-10. Tier 2, Page 1, Byte 1							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
2^3	2^2	2^1	2^0				
10^0 TUNED FREQ.				UNUSED			

1.5.2.7 Example Data Formats

1.5.2.7.1 Monitor Format

Table 1-11 contains examples of data format for full status (Table 1-11b) and partial status (Table 1-11c) monitor operations of a standard WJ-8718 HF Receiver, equipped with the WJ-8718/232 Option. Operating parameters of the receiver to be monitored (at address 15) are given in Table 1-11a.

Table 1-11. Monitor Format

Table 1-11a. Address 15 Receiver Parameters

Tuned Frequency	12.34567 MHz
BFO Frequency	-3.0 kHz
Operating Mode	Local
Bandwidth	3.2 kHz
Gain Mode	Fast AGC
Detection Mode	AM
Signal Strength	Maximum

Table 1-11b. Full Status Monitor

Byte Number	Binary Code	
1	1 1 0 0 1 1 1 1	Controller to Receiver
2	1 1 1 0 0 x x x	Controller to Receiver
3	1 1 0 0 1 1 1 1	Receiver to Controller
4	x x x x 0 0 0 1	Receiver to Controller
5	0 0 1 0 0 0 1 1	Receiver to Controller
6	0 1 0 0 0 1 0 1	Receiver to Controller
7	0 1 1 0 0 1 1 1	Receiver to Controller
8	0 1 0 0 0 0 0 0	Receiver to Controller
9	0 0 1 1 0 0 0 0	Receiver to Controller
10	0 x 1 1 1 1 1 1	Receiver to Controller

Table 1-11c. Bandwidth/Gain Mode/Detection Mode Monitor

Byte Number	Binary Code	
1	1 1 0 0 1 1 1 1	Controller to Receiver
2	1 1 1 0 1 1 0 0	Controller to Receiver
3	1 1 0 0 1 1 1 1	Receiver to Controller
4	0 1 0 0 0 0 0 0	Receiver to Controller

1.5.2.7.2 Command Format

In the example in Table 1-12, the receiver at address 4 is commanded to establish the parameters listed in Table 1-12a. Table 1-12b lists the data format for full status command and Table 1-12c is the data for commanding only the BFO frequency.

Table 1-12. Command Format

Table 1-12a. Command Parameters to Address 4 Receiver

Tuned Frequency	23.45678 MHz
BFO Frequency	+6.0 kHz
Operating Mode	Remote
Bandwidth	16 kHz
Gain Mode	Manual
Detection Mode	CW
RF Gain	Maximum

Table 1-12b. Full Status Command

Byte Number	Binary Code	
1	1 1 0 0 0 1 0 0	Controller to Receiver
2	1 1 1 1 0 x x x	
3	x x x x x 1 1 0	
4	0 0 1 1 0 1 0 0	
5	0 1 0 1 0 1 1 0	
6	0 1 1 1 1 0 0 0	
7	0 0 0 0 1 0 1 0	
8	0 1 1 0 0 0 0 0	
9	0 x 0 0 0 0 0 0	

Table 1-12c. Command BFO Frequency

Byte Number	Binary Code	
1	1 1 0 0 0 1 0 0	Controller to Receiver
2	1 1 1 1 1 0 0 0	
3	x x x x x 1 1 0	
1	1 1 0 0 0 1 0 0	
2	1 1 1 1 1 1 0 1	
3	0 1 1 0 0 0 0 0	

1.5.2.7.3 Access Tier 2 Format

In this example, shown in Table 1-13, assume that the receiver is equipped with the 1 Hz Tuning Option (in addition to the 232 option) and the controller desires to monitor the status of the 10 digit of tuned frequency; assume the receiver is at address 20 and the 10^{0} digit is 6.

Table 1-13. Tier 2 Access Format

Byte Number	Binary Code	
1	1 1 0 1 0 1 0 0	Controller to Receiver
2	1 1 1 0 1 1 1 1	
3	1 1 0 1 0 1 0 0	Receiver to Controller
4	1 1 1 0 0 0 0 0	
5	0 1 1 0 x x x x	

1.6 FUNCTIONAL DESCRIPTIONS

The WJ-8718/232 Option consists of three circuit boards, which contain an Intel 8085A Microprocessor with memory, read-only, write-only, and input/output devices to support the microprocessor. Figure 1-5 is the WJ-8718/232 Block Diagram.

The functional descriptions in paragraphs 1.6.1 through 1.6.5.1.7 concern the microprocessor and the functional areas directly related to the microprocessor. Paragraphs 1.6.5 through 1.6.7 contain functional descriptions of each board in the option and are followed by detailed circuit descriptions in paragraphs 1.7.1 through 1.7.3.

1.6.1 INPUT/OUTPUT PORT

The microprocessor requires an input/output port to communicate with the remote control equipment via the RS-232-C Interface Bus. The I/O port is an integrated circuit on the Asynchronous I/O Board, 232-A3. The integrated circuit is a programmable communications interface through which incoming and outgoing data are processed. The I/O port receives data from the remote control equipment in serial form, converts the data to parallel form, signals the microprocessor that the data are ready to be fetched, and transmits the data to the processor on an 8-bit, bi-directional, three-state bus. In similar manner, the I/O port receives data from the microprocessor on the same time-multiplexed bus, converts the data to serial form, and transmits to the remote control equipment.

1.6.2 MEMORY DEVICES

Memory provides locations to store instructions and data for the microprocessor. The processor deals with 8-bit binary fields and the memory associated with the processor is organized to store eight bits in each location. Data and instructions are stored in memory as 8-bit binary numbers or as numbers that are integral (even) multiples of eight bits: 16 bits, 24 bits, and so on. This characteristic 8-bit field is referred to as a byte. Each byte is stored in a memory location that is numbered to distinguish it from all other locations. The number which identifies a memory location is called its address.

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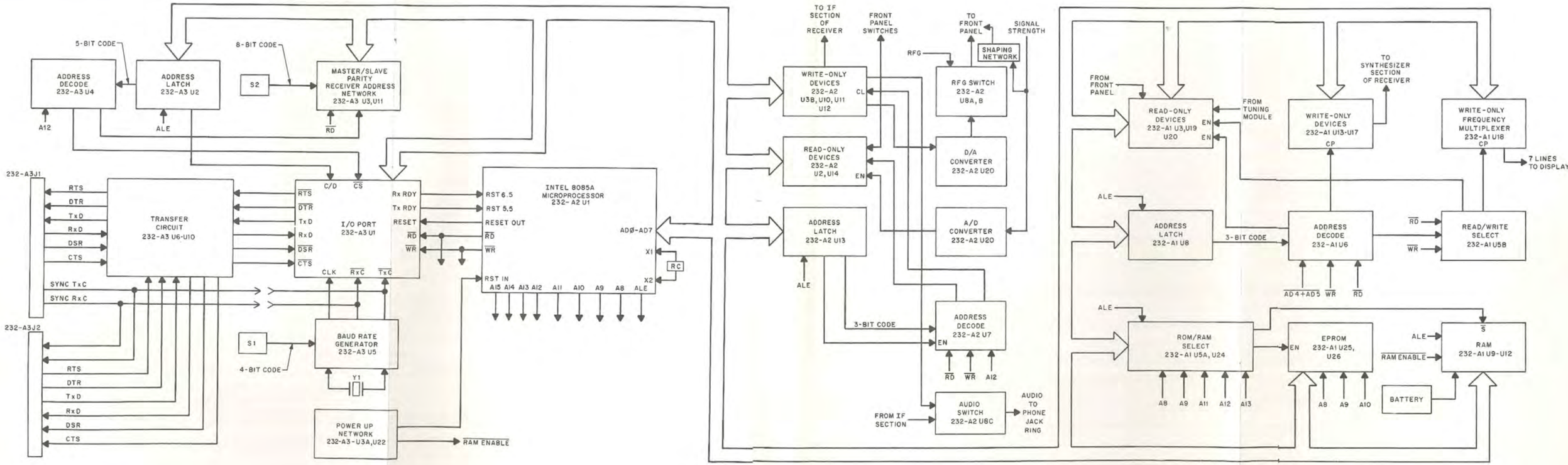


Figure 1-5. WJ-8718/232 Overall Block Diagram

A group of logically related instruction words, or program, is stored in sequential memory locations. The microprocessor reads each instruction in memory in a logically determined sequence and uses it to initiate processing actions. The instruction program is stored in a ROM integrated circuit on the Synthesizer Interface Board, 232-A1.

An addressable area of memory is required to store receiver parameter data so that the data can be accessed for transmission when a remote control equipment request is received, or accessed to be updated as locally or remotely selected receiver parameters are changed. Memory for this purpose is provided by RAM integrated circuits on the Synthesizer Interface Board, 232-A1. The RAM also provides an area of memory which the microprocessor uses as a "scratch pad", to temporarily store data being processed. Another area of RAM is used as a stack, described in paragraph 1.6.4.1.1.

1.6.3 READ-ONLY/WRITE-ONLY DEVICES

Flip-flop and buffer integrated circuits on the 232-A1, 232-A2, and 232-A3 boards serve as addressable read-only and write-only devices. Read-only devices allow the microprocessor to monitor the status of the receiver's front panel controls; write-only devices allow the microprocessor to update receiver parameters.

1.6.4 MICROPROCESSOR

The microprocessor, located on 232-A2, unifies the system by controlling the functions of memory, input/output, read-only, and write-only devices. The processor must be able to access, decode, and execute the binary coded instructions in the program. During the execution of the program, the microprocessor must be able to reference memory, if necessary, and must be able to recognize and respond to signals from the I/O port. The microprocessor meets its obligations by utilizing internal circuits as illustrated by Figure 1-6, Intel 8085A Microprocessor Block Diagram. A brief description of the operation of key functional areas within the microprocessor follows.

1.6.4.1 Registers

Registers are temporary storage units within the microprocessor. Some registers, such as the program counter, flag register, stack pointer, and instruction register have dedicated uses. The accumulator and all other general purpose registers are used for storage of intermediate data during the execution of instructions. The accumulator is also used during arithmetic operations.

1.6.4.1.1 Program Counter and Stack Pointer

The instructions that make up the program are stored in ROM (Read Only Memory) on the 232-A1 board. The microprocessor references the contents of the memory in order to determine what action is appropriate. This means that the processor must know which location contains the next instruction. The processor maintains a register which contains the address of the next program instruction. This register is the program counter. Because the microprocessor updates the program counter each time it fetches an instruction, the program counter is always pointing to the next instruction.

The program is stored in ROM in numerically adjacent addresses (beginning at location zero). The lower order addresses contain the first instructions to be executed and the higher order addresses contain the later instructions. During the course of the instructions, the program may call, or transfer control to, a subroutine. A subroutine is a program within a

FIGURE 1-6 WJ-8718/232

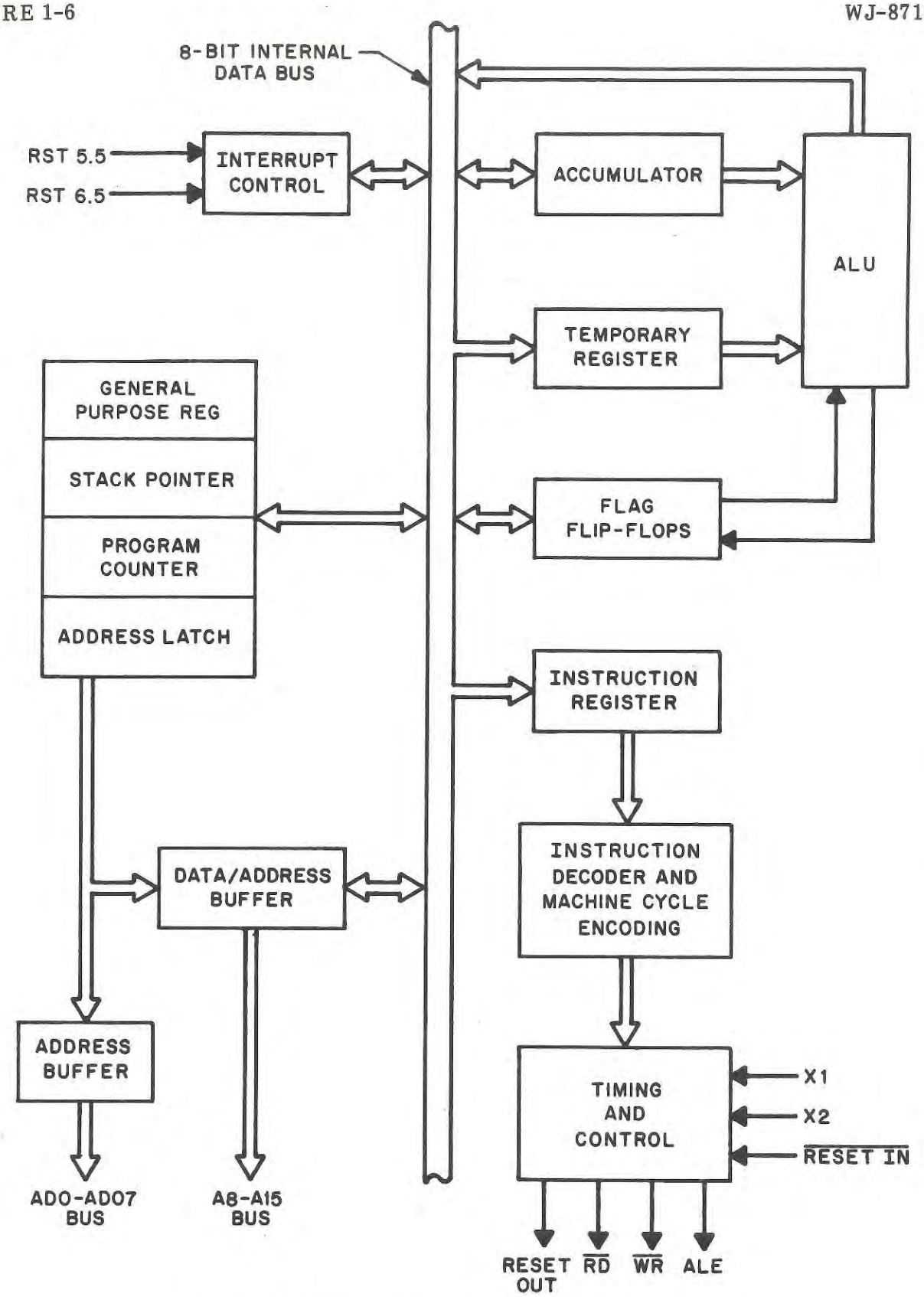


Figure 1-6. Intel 8085A Microprocessor Block Diagram

program; often, it is a general purpose set of instructions which must be executed repeatedly during the program. Memory space is conserved by storing the instructions in an area apart from the main program and directing the processor to this area as necessary. The subroutine instructions are also stored in numerically adjacent addresses in ROM. When a subroutine is called, the processor is instructed to jump to the lowest subroutine address. After the subroutine is finished, the processor must resume execution of the main program; therefore, the processor must remember the contents of the program counter at the time the call occurs.

The microprocessor has a special way of handling subroutines in order to ensure an orderly return to the main program. When the processor receives a call instruction, it increments the program counter and stores the counter's contents in a reserved area in RAM on the 232-A1 board. This memory area is called a stack. The stack saves the address of the instruction to be executed after the subroutine is completed. Next, the processor loads the subroutine address in its program counter, ensuring that the next instruction fetched will be the first step of the subroutine.

The last step of a subroutine is a return. After the processor fetches a return instruction, it replaces the current contents of the program counter with the address on the top of the stack and the program is resumed at the point immediately following the original call instruction.

The processor uses an area of RAM as a stack and maintains an internal pointer register which contains the address of the most recent stack entry. The external stack allows subroutine "nesting", a procedure during which one subroutine calls a second routine.

1.6.4.1.2 Instruction Register and Decoder

Each operation that the microprocessor can perform is identified by a unique byte of data known as an instruction or operation code, generally referred to as an opcode. An 8-bit binary coded word used as an opcode can distinguish between 256 (2^8) alternative actions.

The microprocessor fetches an instruction from memory (ROM) in two distinct operations. First, the processor transmits the address in its program counter to the memory. Next, memory returns the addressed byte to the processor. The instruction byte is stored in a circuit within the processor called the instruction register and is used to direct the activities of the processor during the instruction execution.

The eight bits stored in the instruction register are decoded in the instruction decoder and machine cycle encoding network (Figure 1-5) and are used to activate the output lines of the decoder. The enabled lines are gated by timing signals in the timing and control block to develop electrical signals that initiate specific actions in the processor registers, ALU, and buffers. The outputs of the instruction decoder and internal clock generator provide the state and machine cycle timing signals (paragraph 1.6.4.2).

An 8-bit instruction may not always be sufficient to specify a particular processing action. If more than one byte is used for an instruction, successive instruction bytes are stored in sequentially adjacent memory locations and the microprocessor performs more than one fetch in succession to obtain the full instruction. The first byte retrieved from memory is placed in the instruction register and subsequent bytes are placed in temporary storage internal to the processor; the processor then proceeds with the execution phase.

1.6.4.1.3 Arithmetic Logic Unit (ALU) and Flag Register

The ALU is the portion of the microprocessor hardware which performs the arithmetic and logic operations on the binary data and is inaccessible to the programmer. (An example of the use of the ALU is when the program counter is incremented.)

The flag-bit register is associated with the ALU and the accumulator. The flag-bits specify certain conditions that occur during the course of arithmetic and logical manipulations. The five 8085A Microprocessor flag-bits are carry, auxiliary, sign, zero, and parity. The bits are important to the programmer in establishing the control of processor operation.

1.6.4.2 Internal Clock Generator and Timing

The activities of the microprocessor are cyclical. The processor fetches an instruction, performs the required operations, fetches the next instruction, and so on. This orderly sequence of events requires precise timing. Timing is provided by an internal clock generator with an external RC network providing the reference frequency.

The combined fetch and execution of a single instruction is referred to as an instruction cycle and consists of a series of machine cycles, whose nature is determined by the opcode. The opcode is accessed in the first machine cycle of an instruction cycle. Each machine cycle consists of a series of clock, or timing, cycles determined by the type of instruction being executed and the machine cycle within the instruction cycle.

1.6.4.3 Interrupt Control (RST 5.5 and RST 6.5)

To the microprocessor, an interrupt signal is similar to a subroutine call except that it is initiated externally rather than by the program. High levels on interrupts RST 5.5 and RST 6.5 are generated by the I/O port (USART) on the Asynchronous I/O Board (232-A3) when a data word has been received from or requested by the controller. An interrupt request sets a processor interrupt enable flip-flop; the processor acknowledges the interrupt by suspending the execution of the main program and automatically branches to a subroutine to service the interrupt. The status of the main program is stored on the stack in RAM (paragraph 1.6.4.1.1) until the processor finishes the interrupt service and returns to the main program.

The microprocessor responds to an RST 6.5 interrupt by latching the incoming data into an internal buffer and decoding the data, if necessary. The processor then addresses a location in RAM, issues a write command, transfers the data to the addressed location, and returns to the main program.

The data received by the microprocessor from the remote control equipment following a RST 6.5 interrupt are new parameters for the receiver. During the execution of the main program, the data will be written into addressable flip-flops and transferred to the receiver circuits responsible for effecting the parameter changes.

A high logic level on the RST 5.5 interrupt line tells the microprocessor that the USART is ready to accept a word (from the processor) for transmission. The microprocessor halts execution of the main program and branches to a service routine during which the requested data are transferred from storage to the USART.

1.6.4.4 Data Bus Control Lines ($\overline{RD}$, $\overline{WR}$, ALE)

At the beginning of a fetch machine cycle, the processor places the contents of the program counter (a memory address) on the 16-bit address bus. The high-order byte of address data is placed on the A8 through A16 lines and will remain there for several clock cycles. The low-order byte is placed on the AD0 through AD7 lines and the microprocessor line drivers are enabled. Unlike the upper address lines, the information on the lower address lines will remain there for only one clock cycle after which the drivers will go to their high-impedance state. This is necessary because the AD0 through AD7 lines are multiplexed between the address and data buses. During the first clock cycle of a machine cycle, AD0 through AD7 output the eight lowest bits of the address, after which the lines either output the desired data for a write operation or the drivers will float, allowing the external device to drive the lines for a read operation.

The address information on the AD0 through AD7 lines is transitory, therefore, it must be latched into selected external 8-bit latches. To facilitate the latching of the lowest eight bits of data, the microprocessor provides a special timing signal, Address Latch Enable (ALE), during the first clock state of each machine cycle. After the eight address bits have been latched, the processor initiates either a read or write operation by providing a low level on the $\overline{RD}$ or $\overline{WR}$ control line.

Figure 1-7 illustrates the timing of a read cycle. A low level on the $\overline{RD}$ line enables the addressed memory device and, after a period of time (the access time of the memory), valid data will be present on the AD0 through AD7 lines. The processor next loads the data into its instruction register (paragraph 1.6.4.1.2) and raises $\overline{RD}$ high, disabling the addressed memory device.

After ALE drops, a low level on the $\overline{WR}$ line causes data to be placed on the AD0 through AD7 lines by the processor. The data are loaded into the addressed memory when $\overline{WR}$ goes high. Figure 1-8 illustrates a write timing pulse.

The A8 through A15 data lines are used to identify the MSB's of a memory or I/O location for a data transfer cycle. Selected bits provide enabling pulses to address decode circuits which, in turn, provide enabling pulses to read-only and write-only registers on the 232-A1, 232-A2, and 232-A3 boards. See the detailed circuit descriptions, paragraphs 1.7.1 through 1.7.3 for more details.

1.6.4.5 Reset In/Reset Out

The microprocessor is reset when the RESET $\overline{IN}$ line is low and commences execution of the program when it goes high. The RESET OUT line goes high to reset the 232-A3 communications interface circuit (I/O port).

1.6.5 ASYNCHRONOUS I/O BOARD

The primary function of the Asynchronous I/O Board is to interface the remote control equipment with the microprocessor in the control block of the addressed receiver. An active repeater network on the I/O board facilitates the transfer of status signals and received or transmitted data between equipment via the RS-232-C bus. The network consists of logic gates controlled by the levels of the status signals on the bus. The signal levels are maintained by buffers which regenerate signals that have been degraded by inherent line losses.

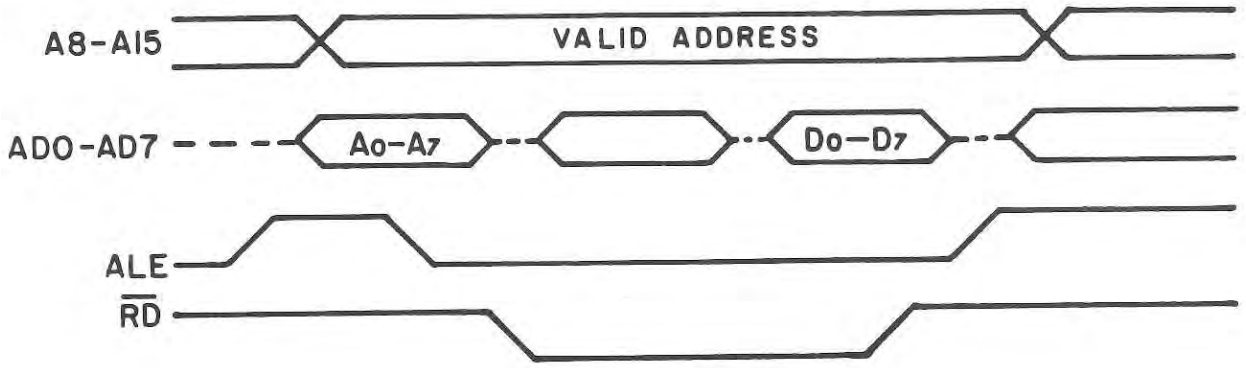


Figure 1-7. $\overline{RD}$ Timing Diagram

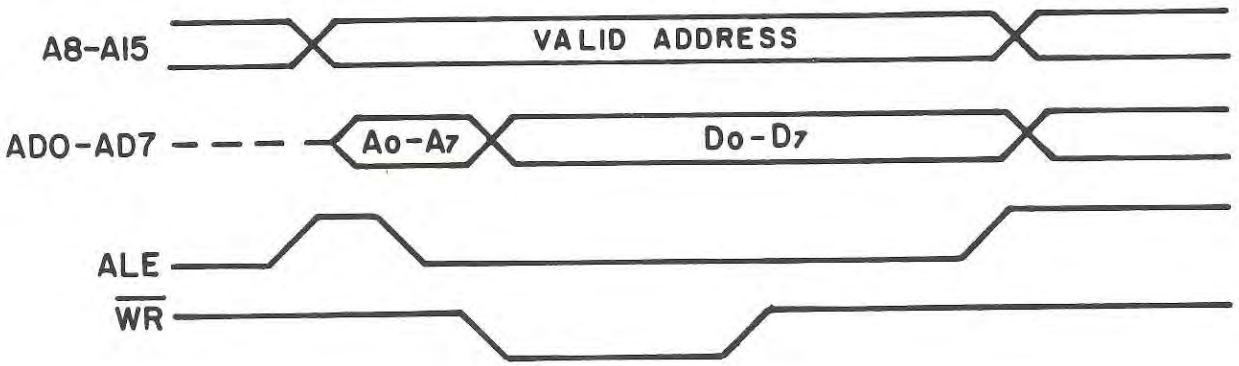


Figure 1-8. $\overline{WR}$ Timing Diagram

An address is established in a receiver to be controlled by entering a valid address code in an I/O board switch assembly (paragraph 1.4.4). The address code is applied to a tri-state buffer which the microprocessor monitors, when it is necessary, to compare the switch-established address with the equipment address on incoming data. If the addresses match, incoming data are accepted and converted to parallel form by the USART for transmission to the microprocessor. The USART also receives parallel data from the microprocessor, converts the data to serial form, signals the remote control equipment, and transmits the data through the active repeater network to the RS-232-C bus.

Operation of the I/O board USART can be asynchronous or synchronous. For asynchronous operation, a programmable divider integrated circuit generates one of 16 switch-selectable frequencies from a crystal controlled input frequency. The frequency generated is determined by the binary-coded logic levels established by opening and closing four I/O board switches.

Synchronous operation is achieved by alternate I/O board connections that permit timing signals from the remote control equipment to be applied to the USART.

1.6.6 IF INTERFACE BOARD

The microprocessor, which is the central control unit of the addressed receiver, is mounted on this board. The microprocessor is reset when the receiver is energized. Immediately, the processor initiates its program at location zero in memory. Following a pre-programmed sequence, the microprocessor proceeds to fetch instructions from sequential memory locations and perform the operations necessary to carry out the instructions. See paragraphs 1.6.4 through 1.6.4.5 for a functional description of processor activities.

In addition to the microprocessor and read/write peripheral devices, the IF Interface Board contains a power-up circuit, D/A and A/D converters (for RF gain and signal strength voltages), and an address decode network.

1.6.7 SYNTHESIZER INTERFACE BOARD

A pre-programmed EPROM integrated circuit on the Synthesizer Board contains 8-bit memory locations from 0000 to 07FF. The instructions for the microprocessor are stored in the EPROM and are read sequentially by the microprocessor.

The microprocessor begins its program by fetching the contents of location 0000 in the EPROM. If the complete instruction is stored in more than one location, the microprocessor stores the contents of 0000 in its own internal registers and returns to the EPROM to read location 0001. The microprocessor continues to fetch and store instructions until it has enough information. A program counter internal to the microprocessor is constantly updated with the addressed memory location. When an instruction is complete, the microprocessor executes the instruction, and returns to the EPROM to fetch the next instruction in the sequence. The procedure continues until the microprocessor is instructed to return to the beginning of the program.

During the course of the program, the microprocessor will read into or write from an addressed peripheral device. During a write instruction, the microprocessor may address RAM or a write-only peripheral device. Six write-only registers on the Synthesizer Interface Board shift received RF and BFO data to the receiver's display section and to the RF and BFO synthesizers. During read programs, the microprocessor monitors the status of front panel

controls. The monitored data are transmitted to the remote control equipment via the I/O board. RAM integrated circuits on the Synthesizer Interface Board are used to store transitory data.

1.7 DETAILED CIRCUIT DESCRIPTIONS

Refer to Figures 1-22 through 1-25, schematic diagrams, to correlate the following circuit descriptions, written in order of the reference designations.

1.7.1 SYNTHESIZER INTERFACE BOARD (232-A1)

The Synthesizer Interface Board replaces the Manual Tuning Up/Down Counter (A6A1) in the WJ-8718 HF Receiver. The board interfaces the microprocessor data bus with receiver front panel controls, BFO and LO Synthesizers, and frequency display through read- and write-only devices. Random Access Memory (RAM) provides temporary storage and Erasable Programmable Read Only Memory (EPROM) contains the microprocessor's instruction program. Figure 1-9 is a simplified block diagram of the 232-A1 board.

1.7.1.1 ROM/RAM Select (U24)

Integrated circuit U24 is a three-to-eight line decoder which is enabled when RAM or ROM is addressed. The decoder provides enable pulses for a RAM select integrated circuit (U5A) or for one of two EPROM's (U25 and U26) by decoding three bits of the high-order hexadecimal coded memory address. ROM 2, U25, is not used in this WJ-8718/232 Option application, but its relationship to U24 will be included in the discussion.

Table 1-14 lists the microprocessor data bus lines and the range of memory addresses decoded by U24. Only three of the eight available U24 outputs are used to provide the low logic levels required to enable U5A, U25, and U26. Table 1-15 is the truth table for the three outputs used: Y0, Y1, and Y2. The logic levels on the enable inputs (G1, G2A, and G2B) and the select inputs (A, B, and C), as listed in the table, are the only combinations of logic level inputs that provide a low logic level on one of the three used output lines. All other input levels produce high levels on the output lines and hold U5A, U25, and U26 in the disabled state.

1.7.1.1.1 U24 Enable

U24 is enabled with one active-high and two active-low logic levels on the G inputs. G1 is tied to +5 Vdc to provide the high level; therefore, the other two enable inputs must be low to enable the decoder. G2A and G2B are tied to microprocessor control line ALE and data line A12, respectively. ALE goes low when a valid address is placed on the microprocessor data bus. Table 1-14 shows that A12 is low when a ROM or RAM address is on the data bus. The A12 line carries the least significant bit of the most significant digit of the memory address. The hexadecimal MSD of all other addressable devices on the data bus is 1 (binary 0001); therefore, A12 is high when any device other than RAM or ROM is addressed.

1.7.1.1.2 U24 Select

When U24 is enabled, the A, B, and C inputs are decoded. The decode inputs carry the A11 (A), A13 (B), and A14 (C) high-order address bits. The decoder must provide a low level on one of the Y outputs:

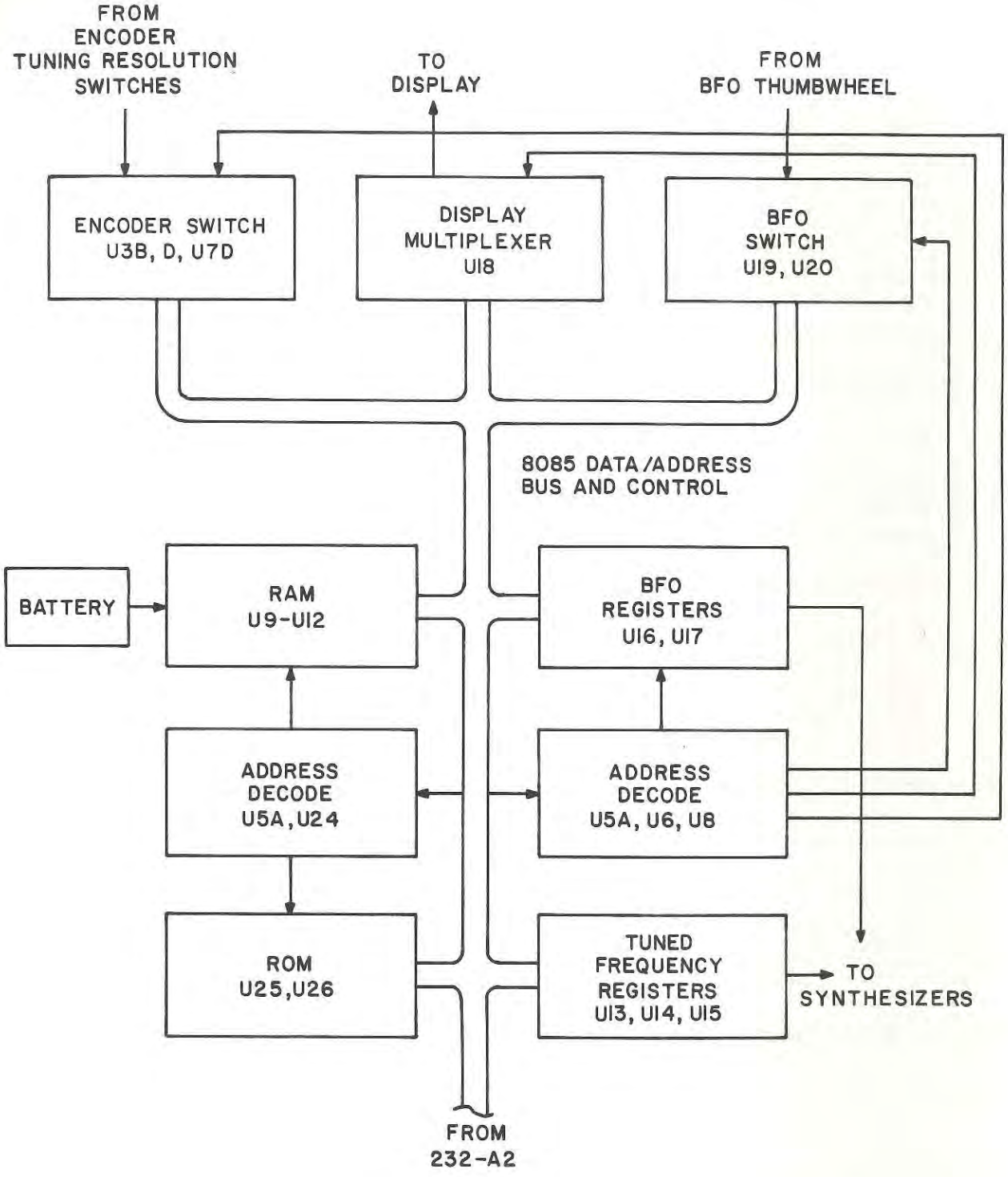


Figure 1-9. Synthesizer Interface Board, Simplified Block Diagram

Table 1-14. RAM/ROM Address Data

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
ROM 1 (U26)				
From 0 0 0 0 =	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
To 0 7 F F =	0 0 0 0	0 1 1 1	1 1 1 1	1 1 1 1
ROM 2 (U25)				
From 0 8 0 0 =	0 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0
To 0 F F F =	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1
RAM 1 (U9, U10)				
From 2 0 0 0 =	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0
To 2 0 F F =	0 0 1 0	0 0 0 0	1 1 1 1	1 1 1 1
RAM 2 (U11, U12)				
From 2 1 0 0 =	0 0 1 0	0 0 0 1	0 0 0 0	0 0 0 0
To 2 1 F F =	0 0 1 0	0 0 0 1	1 1 1 1	1 1 1 1

NOTE: Data Lines 0-7 = AD0-AD7
Data Lines 8-15 = A8-A15

Table 1-15. U24 Truth Table

	Inputs						Outputs		
	Enable			Select					
	G1	G2A	G2B	C	B	A	Y_0	Y_1	Y_2
Signal	+5 V	ALE	A12	A14	A13	A11			
	1	0	0	0	0	0	0	1	1
	1	0	0	0	0	1	1	0	1
	1	0	0	0	1	0	1	1	0
	0	0	0	0	0	0	1	1	1
	0	1	0	0	0	0	1	1	1
	0	0	1	0	0	0	1	1	1

Y0 = 0: enables ROM 1, U26
Y1 = 0: enables ROM 2, U25
Y2 = 0: enables RAM select circuit, U5A

Refer to Table 1-15 (U24 Truth Table) and note the conditions required for Y0 to go low, enabling ROM 1, U26: C = 0, B = 0, A = 0. Table 1-14 (RAM/ROM Address Data) shows that the only time A11 (A), A13 (B), and A14 (C) are low at the same instant is when a hexadecimal number in the address range of ROM 1 (0000 - 07FF), U26, is on the data bus.

Likewise, the U24 truth table shows that Y1 is low, enabling ROM 2, U25 (not used) when C = 0, B = 0, and A = 1. Table 1-14 shows that the only time A14 (C) is low, A13 (B) is low, and A11(A) is high is when a hexadecimal number in the address range of ROM 2 (0800 - 0FFF), U25, is on the data bus.

The truth table indicates that Y2 is low, enabling ROM select circuit U5A, when C = 0, B = 1, and A = 0. Table 1-14 shows that A14 (C) is low, A13 (B) is high and A11 (A) is low only when a hexadecimal number in the address range of RAM (2000 - 21FF) is on the data bus.

1.7.1.2 RAM Select (U5A)

U5A is a two- to four-line decoder enabled by an active-low from the Y2 output of U24. As described in paragraph 1.7.1.1.2, when the U24 decoder senses that RAM address is on the data bus, Y2 goes low. Decoder U5A decodes two bits of high-order memory address to provide a low enabling pulse to one of two Random Access Memories: RAM 1 (U9 and U10) or RAM 2 (U11 and U12). RAM 2 is unused in this WJ-8718/232 Option application, but the relationship of U5A and RAM 2 will be discussed.

Table 1-16, the U5A Truth Table for the two outputs in use, Y0 and Y1, shows the combinations of input logic levels that cause either Y0 or Y1 to go low. All other possible inputs produce high outputs at Y0 and Y1, holding the two RAM's in the disabled state.

Table 1-16. U5A Truth Table

Inputs			Outputs	
Enable EN	Select A	B	Y0	Y1
U24Y2	A8	A9		
0	0	0	0	1
0	1	0	1	0
0	0	1	1	1
1	1	1	1	1

Output Y0 goes low only when both select inputs, A and B, are low. Refer to Table 1-14 and note that data lines A8 (A) and A9 (B) are low at the same instant when a hexadecimal number in the 2000 to 20FF address range of RAM 1 (U9 and U10) is on the data bus.

Output Y1 is low only when A = 1 and B = 0 (see Table 1-16). Table 1-14 shows that a high level on A8 (A) and low level on A9 (B) occur simultaneously when a hexadecimal number between 2100 and 21FF, the address range of RAM 2 (U11 and U12), is on the data bus.

1.7.1.3 Random Access Memory (U9 through U12)

Two addressable read/write memory locations, each consisting of two 256 x 4 CMOS RAM integrated circuits provide storage for 8 bits of data in memory addresses 2000 through 20FF (RAM 1, U9 and U10) and from 2100 through 21FF (RAM 2, U11 and U12). The RAM's are fully static, and may be maintained in any state for an indefinite period of time. To prevent the loss of data, a battery is used to power the RAM's when power is down (paragraph 1.7.1.3.3).

RAM stores current receiver status data and serves as a stack for the microprocessor to temporarily store register information when a program is interrupted.

On-chip latches for the address and data outputs allow the RAM's to be interfaced with the microprocessor data bus. The data output buffers can be forced to a high impedance, allowing the RAM 1 and RAM 2 outputs to share the data bus. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

A RAM address will always be followed by a read or write operation.

1.7.1.3.1 Read Cycle

Table 1-17 is the RAM truth table for a read operation. Figure 1-10 illustrates the RAM timing necessary for a read operation. In the table, the microprocessor data and control lines are listed below the associated RAM input or output; in the figure, the data or control lines are in parentheses after the associated RAM input or output.

The RAM Read cycle is initiated on the falling edge of ALE ($\overline{CE}$). This signal latches the input address word into on-chip registers. After a required hold time, the address lines may change states without affecting device operation. In order to read the output data, ALE ($\overline{CE}$), RAM ENABLE ($\overline{CS2}$), and $\overline{CS1}$ must be low and $\overline{WR}$ (R/$\overline{W}$) must be high. The valid output data are latched into RAM output data latches on the rising edge of ALE and will remain latched until ALE falls. Either or both $\overline{CS1}$ or $\overline{CS2}$ may be used to force the output buffers into a high impedance state.

1.7.1.3.2 RAM: Write Cycle

Table 1-18 is the truth table for RAM during a write cycle. Figure 1-11 illustrates the required RAM write cycle timing pulses. In the table, the microprocessor data and control lines are listed below the associated RAM input or output; in the figure, the microprocessor data and control lines are in parentheses and follow the associated RAM port.

In the write cycle, the falling edge of ALE ($\overline{CE}$) latches the address into on-chip registers. The write portion of the cycle is when $\overline{CE}$, R/$\overline{W}$, $\overline{CS1}$, and $\overline{CS2}$ are low simultaneously and is terminated by the first rising edge of $\overline{CE}$, R/$\overline{W}$, $\overline{CS1}$ or $\overline{CS2}$.

Data multiplexing is done internal to the chip and is controlled by $\overline{WR}$. When $\overline{WR}$ (R/$\overline{W}$) goes low, the output buffers are forced to a high impedance state. After an output disable time, input data are placed on the bus.

Table 1-17. RAM: Read Cycle

	INPUTS					OUTPUTS	
Time Reference	$\overline{CE}$ ALE	$\overline{CS1}$ U5AY0/Y1	$\overline{CS2}$ $\overline{RAM\ EN}$	R/$\overline{W}$ $\overline{WR}$	A0-7 AD0-7	I/O1-4 AD0-7	Function
-1	H	H	H	X	X	Z	Memory Disabled
0	↓	X	X	H	V	Z	Cycle Begins, Addresses are Latched
1	0	0	0	H	X	X	Output Enabled
2	0	0	0	H	X	V	Output Valid
3	↑	0	0	H	X	V	Output Latched
4	H	H	H	X	X	Z	Device Disabled, Prepare for Next Cycle (same as -1)
5	↓	X	X	H	V	Z	Cycle ends, Next Cycle Begins (same as 0)

NOTES:
1. Device selected only if $\overline{CS1}$ and $\overline{CS2}$ are both low, disabled if either $\overline{CS1}$ or $\overline{CS2}$ is high.
2. Z = high impedance, V = valid, X = don't care.
3. ↓ = falling edge, ↑ = rising edge.

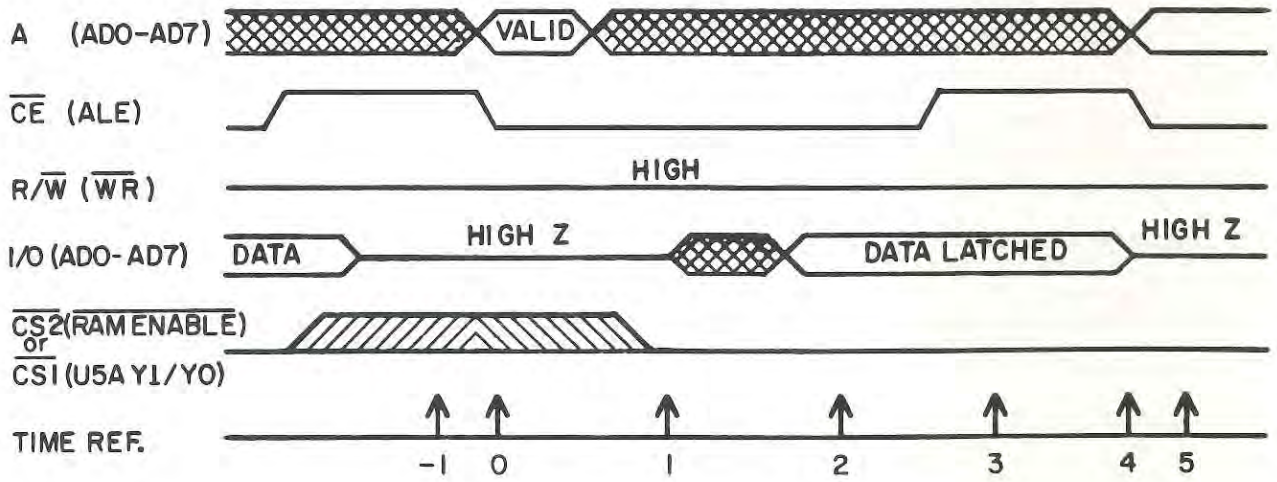


Figure 1-10. Read Cycle Timing Diagram (RAM)

Table 1-18. RAM: Write Cycle

INPUTS						OUTPUTS	
Time Reference	$\overline{CE}$ ALE	$\overline{CS1}$ U5AY0/Y1	$\overline{CS2}$ RAM EN	R/$\overline{W}$ $\overline{WR}$	A0-7 AD0-7	I/O1-4 AD0-7	Function
-1	H	H	H	X	X	Z	Memory Disabled
0	↓	X	X	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	L	L	X	Z	Write Period Begins
2	L	L	L	L	X	V	Data In are Written
3	↑	X	X	H	X	Z	Write is Completed
4	H	H	H	X	X	Z	Prepare for Next Cycle (same as -1)
5	↓	X	X	X	V	Z	Cycle Ends, Next Cycle Begins (same as 0)

NOTES:
1. Device selected only if $\overline{CS1}$ and $\overline{CS2}$ are both low, disabled if either $\overline{CS1}$ or $\overline{CS2}$ is high.
2. Z = high impedance, V = valid, X = don't care.
3. ↓ = falling edge, ↑ = rising edge.

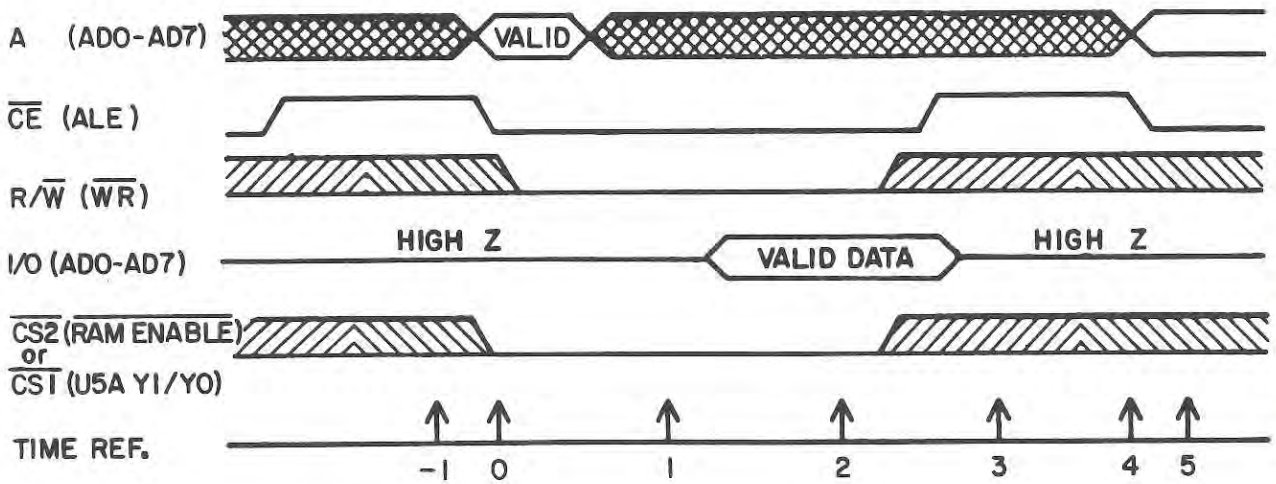


Figure 1-11. Write Cycle Timing Diagram (RAM)

1.7.1.3.3 Battery Backup

An inherent quality of RAM is that it is volatile, meaning that data are not held when power is removed. To prevent the loss of data, a battery (BT1) is used to power the RAM's when power is down.

Diode CR1, forward biased by Vcc when power is on, charges the 2.4 V battery through R5. When power is down, Vcc drops to zero and diode CR1 becomes reverse biased, allowing current to flow only to the RAM circuits connected to Vcc2.

1.7.1.4 Read-Only Memory (U25, U26)

The Synthesizer Interface Board houses two 16,384-bit ultraviolet erasable and electrically programmable read-only memories (EPROM's). In this WJ-8718/232 Option application, only ROM 1 (U26) is used. ROM 2 (U25) is available if future design considerations warrant the need for expanded read-only memory.

Prior to shipment, the EPROM is programmed with the microprocessor instruction data. Before programming, all bits in the EPROM are in state 1. Data are introduced by selectively programming 0's into the desired bit locations. The only way a 0 can be changed to a 1 is through ultraviolet erasure.

Erasure begins to occur when the EPROM window is exposed to light with wavelengths shorter than approximately 4000 Angstroms. Because sunlight and certain types of fluorescent lamps have wavelengths in the 3000 to 4000 Angstroms range, an opaque label is placed over the window to prevent unintentional erasure.

1.7.1.4.1 EPROM Operation

Power required for the operation of the EPROM is +5 Vdc. The programmed read-only memory device, U26, has two modes of operation: read and standby. All inputs to the device are TTL levels.

1.7.1.4.2 Control Inputs

The $\overline{CE}$ input to U26 is a chip-select pulse from RAM/ROM select circuit U24. The low enable pulse is provided when decoder U24 senses that the hexadecimal coded address on the microprocessor data bus is in the range of 0000 through 07FF. The microprocessor addresses location 0000 at power-up and consecutively reads and executes the instructions stored in EPROM.

The OE input is tied to the microprocessor $\overline{RD}$ signal, which is pulled low when the processor initiates a read operation. Output Enable (OE) is used to take the outputs out of tri-state.

1.7.1.4.3 Read Mode

When the microprocessor initiates a read operation, the 16-bit memory address is placed on the data bus, ALE goes low, and if the memory addressed is RAM or ROM, U24 is enabled. If the hexadecimal coded address is between 0000 and 07FF, U24 pulls the U26 Chip Enable ($\overline{CE}$) line low, and the AD0 through AD7 address bits (from low-order address latch, U8) and the A8, A9, and A10 address bits are applied to the EPROM device through Address Inputs A0 through A10. After an address access time, followed by the falling edge of the

microprocessor $\overline{RD}$ signal, the data stored in the addressed memory location are available at the O0 through O7 EPROM Data Outputs.

The data are loaded on the AD0 through AD7 address/data bus lines and latched into the microprocessor's internal instruction register (paragraph 1.6.4.1.2), on the rising edge of $\overline{RD}$.

1.7.1.4.4 Standby Mode

The EPROM device is in reduced power standby mode when the $\overline{CE}$ line is held at TTL high logic level. During the standby mode, the outputs are at a high impedence state, independent of the OE input, allowing the shared data bus to be driven by other devices addressed for a read operation.

1.7.1.5 Low-Order Address Latch (U8)

U8 is an octal D-type flip-flop. The clear ($\overline{CLR}$) input is wired high, causing information at the D inputs to transfer to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect or the output. The clock input to U8 is the microprocessor control line ALE which is inverted by U4C. The output of NAND gate U4C goes high when ALE goes low. ALE transitions to a low when a valid address is on the data bus.

When the address on the AD0 through AD7 and A8 through A15 lines of the data bus is not a RAM address, the Input/Output and data ports of U9 through U12 present a high impedence to the address bus which is gated through the buffer network composed of U1 (A, B, D, E, and F) and U2 (D, E, and F) to the D inputs of U8. The positive-going output of U4C gates the 8 lower-order address bits from the D inputs to the Q outputs of U8.

If EPROM 1 (U26) has been addressed, a low level at the enable ($\overline{CE}$) input takes the U26 outputs out of tri-state, the addressed memory location is accessed, and the data contained in that location are gated to the U26 outputs. If U26 has not been addressed, a high level at $\overline{CE}$ tri-states the output, preventing the levels at the A inputs from affecting the outputs of the device.

Three of the Q outputs of U8 are tied directly to the select inputs of U6 and two others are gated to the enable inputs of U6; these five binary coded bits of lower-order address data, plus the $\overline{RD}/\overline{WR}$ lines and the A12 address bit, allow U6 to select and enable one of seven read-only and write-only devices on the Synthesizer Interface Board.

1.7.1.6 RD/WR Select (U6)

U6 is a three-to-eight line decoder. Table 1-19 is the U6 Truth Table. To decode the three select bits at A, B, and C, the decoder must be enabled by one active-high and two active-low logic levels on the G inputs.

1.7.1.6.1 U6 Enable

Decoder U6 provides an enabling pulse for each of nine read-only or write-only devices on the Synthesizer Interface Board; therefore, U6 must be enabled when any one of the nine devices is addressed for a read or write operation. The addresses for the nine devices are hexadecimal numbers from 1030 through 1037 (1037 addresses both a read and a write

device). Table 1-20 lists the binary coded addresses and the data line that carries each bit. The enable inputs are provided as follows:

1. A high logic level is provided at G1 by A12. Refer to Table 1-20 and note that A12 is high when any address in the hexadecimal 1030 through 1037 range is on the bus.

2. A low logic level is applied to G2A when the bits carried by AD4 and AD5 enable U4D. The output of U4D is low only when both inputs are high. Table 1-20 shows that both AD4 and AD5 are high when any address in the 1030 through 1037 range is on the bus.

3. A low logic level is applied to G2B from the output of inverter U4B when the input to U4B (the output of U4A) is high. U4A has a high output level when either input is low; the inputs are tied to the $\overline{RD}$ and $\overline{WR}$ microprocessor control lines, one of which goes low to initiate a read or write operation.

1.7.1.6.2 U6 Select

The A, B, and C select inputs to U6 are the three least significant bits of address on the data bus, and are carried on the AD0, AD1, and AD2 data lines. Table 1-20 illustrates the logic levels of the three LSB's in the hexadecimal address range from 1030 through 1037. Refer to Table 1-19 (U6 Truth Table) and note that as the count on the select inputs proceeds from 000 through 111, each increment causes one Y output to go low. Seven of these Y outputs are applied to clock a read or write device (described in paragraphs 1.7.1.7 and 1.7.1.10) and the eighth is used to enable U5B (described in paragraph 1.7.1.8).

1.7.1.7 Frequency Registers (U13 Through U17)

U13 through U17 are octal D-type flip-flops and are identical to U8, described in paragraph 1.7.1.5. The registers serve the microprocessor in a write-only capacity and provide the current RF and BFO frequency data to the receiver synthesizer circuits. Table 1-20 lists the register addresses.

The clock input to each register is tied to one Y output of decoder U6. When an address in the hexadecimal range of 1030 through 1034 is on the data bus, U8 is clocked by the falling edge of ALE, U6 is enabled by the data in U8, and the clock pulse to the addressed register goes low (paragraph 1.7.1.6.2). The microprocessor loads the frequency data to be written into the addressed register on the data bus and $\overline{WR}$ goes from low to high, causing U6 to be disabled by the high level at G2B, and the Y outputs of U6 go high. The U6 outputs that already were high do not change, but the one low output goes high. This low-to-high transition on the clock input to the addressed register causes the frequency data to be transferred from the D inputs to the Q outputs and applied to the receiver LO and BFO Synthesizers.

The 8-bit RF frequency data words are provided in Table 1-21 and the 8-bit BFO frequency data words are provided in Table 1-22.

1.7.1.8 Read/Write Address 1037 Select (U5B)

Decoder U5B is enabled by a low logic level pulse at EN2 from the U6Y7 output. As shown in Tables 1-19 and 1-20, the low level at U6Y7 occurs when the 1037 address is on the

data bus. The select inputs to U5B are at A2 and B2, tied to the microprocessor control lines $\overline{RD}$ and $\overline{WR}$, respectively.

Table 1-19. U6 Truth Table

Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

Table 1-20. Addresses 1030 Through 1037

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U13	0 0 0 1	0 0 0 0	0 0 1 1	0 0 0 0
U14	0 0 0 1	0 0 0 0	0 0 1 1	0 0 0 1
U15	0 0 0 1	0 0 0 0	0 0 1 1	0 0 1 0
U16	0 0 0 1	0 0 0 0	0 0 1 1	0 0 1 1
U17	0 0 0 1	0 0 0 0	0 0 1 1	0 1 0 0
U20	0 0 0 1	0 0 0 0	0 0 1 1	0 1 0 1
U19	0 0 0 1	0 0 0 0	0 0 1 1	0 1 1 0
U3 (B,D)	0 0 0 1	0 0 0 0	0 0 1 1	0 1 1 1
U18	0 0 0 1	0 0 0 0	0 0 1 1	0 1 1 1

NOTE: Data Lines 0-7 = AD0-AD7
Data Lines 8-15 = A8-A15

Table 1-21. RF Frequency Data Words

Frequency Digit	10^1	10^2	10^3	10^4	10^5	10^6	10^7
Frequency Bits	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0-2^3	2^0, 2^1
Register Outputs	Q7-Q4	Q3-Q0	Q7-Q4	Q3-Q0	Q7-Q4	Q3-Q0	Q7, Q6
Register	U13	U13	U14	U14	U15	U15	U16

Table 1-22. BFO Frequency Data Words

Frequency Data	Sign		Frequency Digit		
	+	-	10^1	10^2	10^3
Frequency Bit			2^3-2^0	2^3-2^0	2^3-2^0
Register Outputs	Q5	Q4	Q3-Q0	Q7-Q4	Q3-Q0
Register	U16	U16	U16	U17	U17

Table 1-23, the U5B Truth Table, shows that the Y1 output goes low when $\overline{RD}$ is low and the Y2 output goes low when $\overline{WR}$ is low. At all other times, both outputs are at a high logic level. Y1 is the clock input to register U18, described in paragraph 1.7.1.9 and Y2 is the enabling pulse to tri-state buffers U3 (B and D) and U20, discussed in paragraph 1.7.1.10.

Table 1-23. U5B Truth Table

Inputs			Outputs	
Enable	Select			
EN2, (U6Y7)	A2 ($\overline{RD}$)	B2 ($\overline{WR}$)	Y1	Y2
L	H	L	L	H
L	L	H	H	L

1.7.1.9 RF Frequency Multiplexer (U18)

The RF frequency display is software multiplexed through U18 and is updated by the microprocessor periodically each time the program is executed. U18 is an octal flip-flop identical to U8, described in paragraph 1.7.1.5. The clock input to U18 transitions low when $\overline{WR}$ is low and address 1037 is on the data bus. The microprocessor loads the RF frequency data on the data bus and $\overline{WR}$ goes high, disabling U5B. The Y1 output of U5B goes high; this low-to-high transition at the U18 clock input transfers the frequency data from the D inputs to the Q outputs.

The frequency information on the data bus is in binary-coded word form and consists of a 3-bit RF frequency digit code and four bits of RF frequency data. The Q0, Q1, and Q2 outputs are decoded on the display board to determine which digit of RF frequency data is on the Q3 through Q6 lines. For example, if the Q1, Q2, and Q3 lines are 0, 0, and 0, four bits of 10^1 digit of RF frequency are on the Q3 through Q6 lines. Table 1-24 lists the binary codes for the seven bits of frequency data applied to the Frequency Display board from J2 of the Synthesizer Interface Board.

Table 1-24. Frequency Display Data Word

Q0	Q1	Q2	2^3 2^2 2^1 2^0
0	0	0	10^1 digit
1	0	0	10^2 digit
0	1	0	10^3 digit
1	1	0	10^4 digit
0	0	1	10^5 digit
1	0	1	10^6 digit
0	1	1	10^7 digit
1	1	1	Not Used

1.7.1.10 Read-Only Devices (U3B, D, U7, U19, U20)

By addressing one of the Synthesizer Interface Board read-only devices (U3B, D, U7, U19, or U20) and issuing a $\overline{RD}$ signal, the microprocessor can read the status of Tuning Module A7 and the receiver front panel controls and switches.

1.7.1.10.1 BFO Frequency/Sign (U20)

The microprocessor addresses location 1035 to read the front panel 10^1 BFO frequency (when the receiver is equipped with the WJ-8718/10 Hz BFO option), the BFO sign, and the encoder direction and clock status.

The Y5 output of U6 goes low when the 1035 address is on the data bus, causing the enable inputs to U20 to go low. When the microprocessor issues the $\overline{RD}$ command, the Y5 line goes low enabling U20, a tri-state buffer. The logic levels on the BFO 10^1 frequency digit and the +/- BFO sign thumbwheel switches appear at the outputs of U20 and are placed on the data bus to be read by the microprocessor. Table 1-25 is the address 1035 data word.

Table 1-25. Address 1035 Data Word							
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
2^3	2^2	2^1	2^0	P	M	D	C
10^1 BFO Frequency				See Notes			

NOTES: P(1) = + BFO
M(1) = - BFO
D(1) = Positive Tuning Direction
C = Tuning Encoder Clock

1.7.1.10.2 Encoder Clock/Direction

The encoder direction and clock data are read by the microprocessor when the U6Y5 line goes low (a result of address 1035 on the data bus). The U6Y5 line is tied to the OD (Output Disable) inputs to U7 (pins 1 and 2). U7 is a dual flip-flop with tri-state outputs tied to the data bus. As long as the OD inputs are high, the Q outputs are tri-stated; when U6Y5 goes low, the outputs are enabled. Paragraph 1.7.1.10.4 contains information about clearing the Tuning Encoder data.

1.7.1.10.3 BFO Frequency

Tri-state buffer U19 is enabled by a low logic level from U6Y6, after 1036 is addressed and the $\overline{RD}$ line goes low. Enabling U19 takes the outputs out of tri-state and the microprocessor can read the logic levels on the front panel BFO frequency (10^2 and 10^3 digits) thumbwheel switches, as shown in Table 1-26. Table 1-26 is the Address 1036 Data Word.

Table 1-26. Address 1036 Data Word							
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
10^3 BFO Frequency				10^2 BFO Frequency			

1.7.1.10.4 Clear Tuning Encoder Data

An additional function of address 1036 is provided by applying the resultant low logic level at U6Y6 to the enable input of tri-state buffer U3A (pin 1). When U3A is enabled, the high logic level at pin 2 is transferred to the output, clearing flip-flop register U7 (outputs go low).

1.7.1.10.5 Operating Mode/Tuning Resolution (U3B, D)

The positive-to-negative transition of the Y2 output of U5B occurs when $\overline{RD}$ goes low after the 1037 address has been placed on the data bus. Tri-state buffers U3B and D are

enabled and the lines at J4, pins 13 and 16, provide a common return for the front panel tuning resolution (RF frequency) pushbuttons and the tuning disable control, so that the data bus line connected to a switch through J4 will appear as a low level on the line when that particular switch is engaged. Table 1-27 is the address 1037 (Read) Data Word (AD5, AD6, and AD7 are not used).

Table 1-27. Address 1037 (Read) Data Word

AD4	AD3	AD2	AD1	AD0
Remote	10 kHz	1 kHz	100 Hz	10 Hz

1.7.2 IF INTERFACE BOARD (232-A2)

The IF Interface Board replaces the Front Panel Interconnect (A2) in the WJ-8718 HF Receiver when the WJ-8718/232 Option is installed. The Intel 8085A Microprocessor (232-A2U1) coordinates the functions of the WJ-8718/232 Option to provide signals that activate the appropriate devices in the IF and Synthesizer sections of the receiver, allowing receiver parameters to be established when selected in either the remote or local operating mode. The devices on the IF Interface Board also allow the microprocessor to read the status of the front panel switches associated with the IF functions. These functions include gain mode, bandwidth, detection mode, RF gain, signal strength, and phone level. The IF Interface Board also switches the audio at the front panel phones jack from combined audio to single sideband audio in the ISB detection mode.

The IF Interface Board is powered by regulated voltages of +5, -15, and +15 Vdc and an unregulated 10 Vdc. The capacitive network formed by C1 through C10 and C20 prevents ac ripple and voltage spikes. A special power-up network (paragraph 1.7.2.2), built around timer U22, provides the necessary time delay to reset the microprocessor.

Refer to Figure 1-12, the simplified block diagram, and to Figure 1-23, the IF Interface Board Schematic Diagram, to correlate the following detailed circuit descriptions.

1.7.2.1 Microprocessor (U1)

The Intel 8085A Microprocessor is an 8-bit central processing unit. The microprocessor is designed with N-channel technology and requires a single +5 V supply. Basic clock speed is 3 MHz. An external RC network, composed of R35, C11, and C12, drives the internal clock.

The microprocessor contains 12 eight-bit registers. Four registers function as two 16-bit register pairs and six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. Paragraph 1.6.4.1 contains functional descriptions of the microprocessor registers.

A multiplexed data bus allows the microprocessor to communicate with external devices. The execution of the microprocessor program consists of a series of machine cycles and each machine cycle contains a series of clock cycles. During the first clock cycle of a machine cycle, an external device address is placed on the data bus. The address is split between the higher-order 8-bit address bus (A8 through A15) and the lower-order 8-bit address/data bus (AD0 through AD7). The eight lower-order address bits are latched into external devices by the Address Enable Signal (ALE). During the remaining portion of the machine cycle, the bus is used for data.

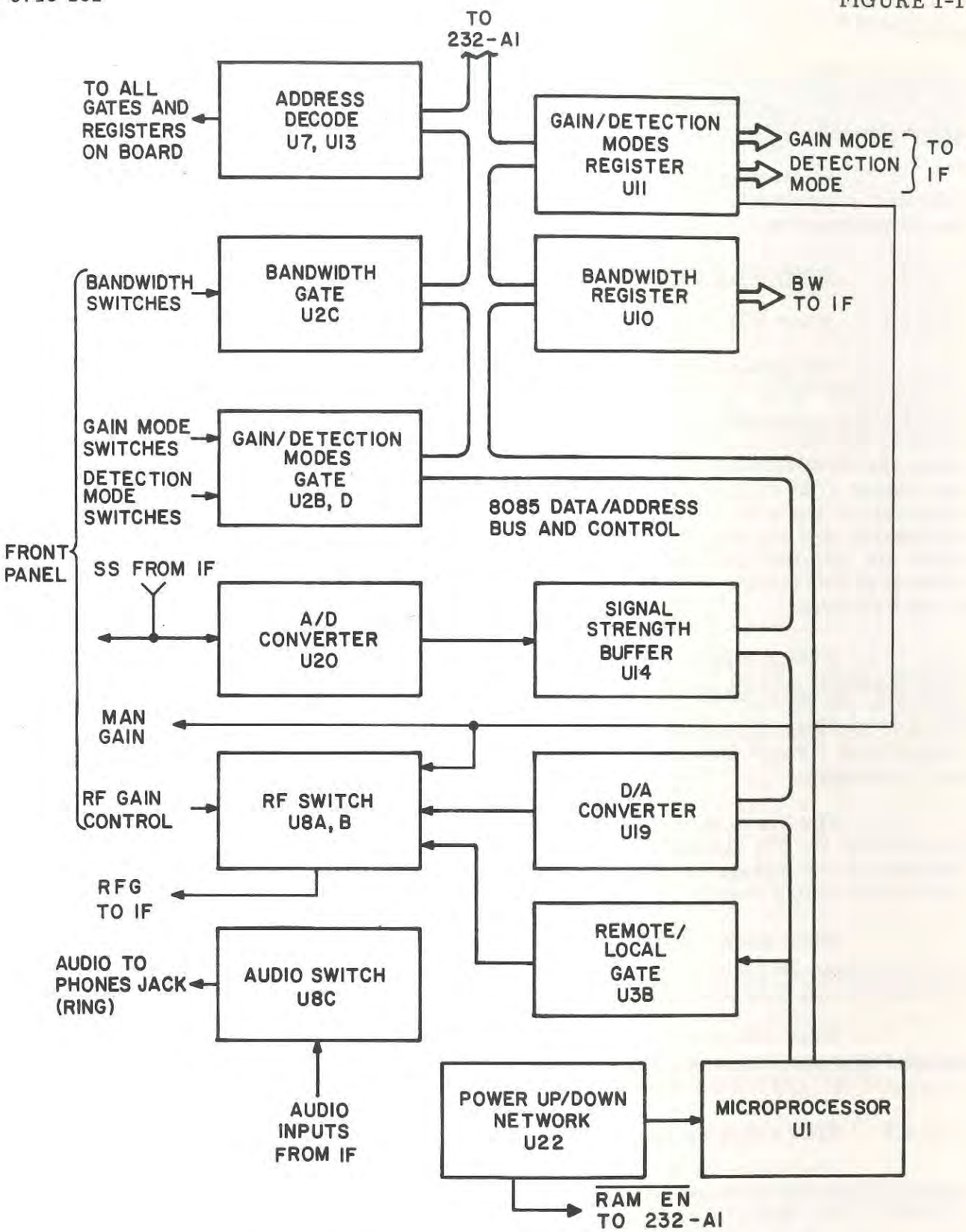


Figure 1-12. IF Interface Board, Simplified Block Diagram

The microprocessor provides $\overline{RD}$, $\overline{WR}$, S_0, S_1 and IO/M signals for bus control. In this WJ-8718/232 application, only the $\overline{RD}$ and $\overline{WR}$ signals are used. Likewise, five interrupt signals are available but the RST 5.5 and RST 6.5 are the only interrupt signals used.

All microprocessor input and output signals used in the WJ-8718/232 Option are described in paragraphs 1.6.4.3, 1.6.4.4, and 1.6.4.5. Figure 1-6 is a functional block diagram of the microprocessor.

1.7.2.2 Power-Up Network

1.7.2.2.1 Timer U22

The power-up network for the microprocessor is designed around timer U22, shown in functional block diagram form in Figure 1-13. The timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistive divider network. The resistive divider is used to set the comparator levels. Because the three resistors are of equal value, the threshold (TH) comparator is referenced internally at 2/3 of supply voltage level and the trigger (TR) comparator is referenced at 1/3 of supply voltage. The outputs of the comparators are tied to the bistable flip-flop (internal) so that a high output from the TH comparator sets the flip-flop (output goes high) and a high output from the TR comparator resets the flip-flop (output goes low). In this application, the configuration of components external to U22 is such that the ratio of the threshold and trigger voltages determines the state of the U22 output.

When power is applied to the receiver, a regulated potential of +5 Vdc is applied to the base of Q1 and to the enabling (R) and VCC inputs to U22. An unregulated +10 Vdc is applied to the emitter of PNP transistor Q1 across emitter resistor R26, Q1 is forward biased, and current flows through R25, R26, CR5, CR6, and Q1. R26 is adjustable to establish the current level through R25. The current through R25 and the resistance value of R25 determine the TR voltage.

The TH voltage is always two diode (CR5 and CR6) drops, approximately 1.4 volts, greater than the TR voltage. As current through the Q1 network increases, the two voltages increase; as the voltages increase, although the voltage difference remains 1.4 volts, the ratio between the voltage levels decreases.

When power is applied and current begins to flow through the Q1 network, the TR and TH voltage levels increase until the ratio of TH to TR voltage becomes less than two-to-one, the U22 flip-flop is reset, and the output at pin 3 of U22 goes low.

When power is interrupted, as the 10 volt potential decreases, the TR and TH voltages decrease until the ratio of TH to TR voltage become greater than two-to-one, the U22 flip-flop is set, and the level at pin 3 of U22 goes high.

1.7.2.2.2 Time Delay Network

Transistor Q2 is turned on by a high output from U22 and is turned off by a low output. When the NPN transistor is on, voltage at the collector is low. This low level is the RST $\overline{IN}$ input to the microprocessor and causes the processor to enter a reset state which lasts as long as RST $\overline{IN}$ is low.

The microprocessor employs a special internal circuit to increase its speed. This circuit, a substrate bias generator, creates a negative voltage which is used to negatively bias

the substrate. The internal circuit, consisting of an oscillator and a charge pump, requires a certain amount of time to stabilize after power is applied. Initially, the RST $\overline{IN}$ line is high (+5 V on the Q2 collector) but as soon as Q2 is turned on, the collector voltage goes low. The time constant of the RC network formed by CR4 and R16 holds the RST $\overline{IN}$ line low for the time period required to stabilize the internal circuits of the microprocessor.

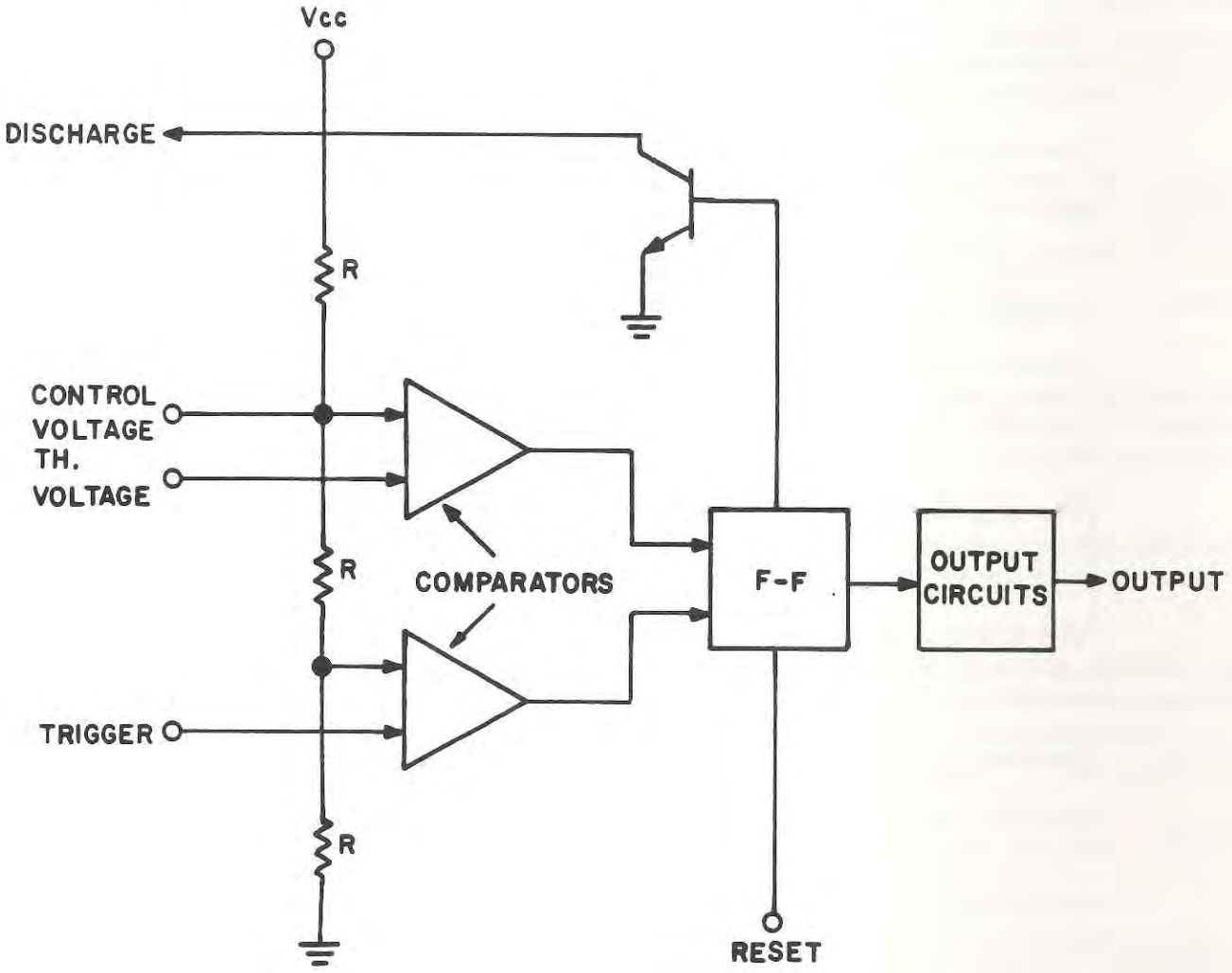


Figure 1-13. Timer U22, Functional Block Diagram

1.7.2.2.3 Ram Enable Flip-Flop (U3A)

The CL (Clock) and D (Data) inputs to U3A are tied to +5 Vdc; therefore, the flip-flop output level is independent of the clock and responds only to the S (Set) and R (Reset) inputs.

After the time delay established by C13 and R16, the RST $\overline{IN}$ signal reaches a high logic level and, a clock pulse later, the microprocessor pulls the RESET OUT signal low. The inversion of the RST $\overline{IN}$ and RESET OUT signals by U4C and U4E, respectively, causes a high

level at the reset input and a low level at the set input to U3A; this condition resets the flip-flop and the Q output goes low. The low level on the RAM ENABLE line enables the RAM devices on the Synthesizer Interface Board, 232-A1, and the microprocessor begins to execute the program stored in Ram location 0000.

1.7.2.3 Address Latch (U13)

The ALE signal goes low to indicate that a valid address is on the AD0 through AD7 bus lines. The ALE signal is inverted by U4C and the resultant positive-going edge is applied to the CP (Clock Pulse) input to U13, an octal flip-flop.

The data at the D inputs of U13 are latched to the Q outputs on the positive-going edge at CP. Three of the Q outputs, the least significant bits of the lower-order address, are the select inputs to U7 and two other address bits are gated to become the enabling pulses to U7, described in the following paragraph.

1.7.2.4 Address Decoder (U7)

Table 1-28 is the truth table for U7. The decoder is enabled when a high logic level and two low logic levels are applied to the G1, G1A, and G2B inputs, respectively. When enabled, U7 provides a low logic level on one of the seven Y outputs based on the coded inputs at A0, A1, and A2.

The input levels listed in Table 1-28 are the only input conditions that result in a low-level output on any of the Y0 through Y6 outputs. All other input conditions result in high levels on each of the Y0 through Y6 outputs (Y7 is unused).

The Y outputs of U7 are the clock and enable inputs to the read-only and write-only devices on the IF Interface Board. Table 1-29 lists the addresses of the devices and the data bus lines that carry each address bit.

1.7.2.4.1 Decoder (U7) Enable

Decoder U7 is enabled with a high and two low logic levels on the enable inputs, G1, G2A, and G2B, respectively.

A high logic level appears at the G1 input when the address bit on the A12 bus line is high. As shown in Table 1-29, the level of the address bit on the A12 line is high during the time that an address in hexadecimal 1xxx is on the bus.

The enable input at G2A (the output of AND gate U21D) goes low only when the $\overline{RD}$ or $\overline{WR}$ signal is low; the $\overline{RD}$ or $\overline{WR}$ signal is low when the microprocessor initiates a read or write operation.

The enable input at G2B is the inverted (by U4F) output of AND gate U21C. The inputs to U21C are derived from the AD4 and AD5 data/address lines. If G2B is to go low, both inputs to U21C must be high. Because the AD5 bit is inverted by U4E prior to reaching the U21C input, the U21C inputs are high only when the latched address bit from the AD5 line is low and the latched AD4 bit level is high. Table 1-29 shows that this condition (AD5, low: AD4, high) occurs when an address in the hexadecimal range from 1010 to 1016 is on the bus.

1.7.2.4.2 Decoder (U7) Select

The select inputs to U7 (A0, A1, and A2) are the three least significant bits of the address latched by U13. As shown in Table 1-28, a Y output goes low only when U7 is enabled and a particular 3-bit code is on the select inputs. Comparison of the select input codes listed in Table 1-28 with the three least significant bits of the addresses listed in Table 1-29 shows that one of the Y0 through Y6 outputs goes low when one of the addresses in the hexadecimal 1010 through 1016 range is on the bus. Each Y output is tied to an enable input of a read-only device or the clock input of a write-only device on the IF Interface Board (232-A2).

Table 1-28. U7 Truth Table

Inputs						Outputs						
Enable			Select									
G1	G2A	G2B	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6
H	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H
H	L	L	L	H	H	H	H	H	H	H	H	L

Table 1-29. Addresses 1010 Through 1016

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U3B	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 0
U10	0 0 0 1	0 0 0 0	0 0 0 1	0 0 0 1
U11	0 0 0 1	0 0 0 0	0 0 0 1	0 0 1 0
U12	0 0 0 1	0 0 0 0	0 0 0 1	0 0 1 1
U14	0 0 0 1	0 0 0 0	0 0 0 1	0 1 0 0
U2B	0 0 0 1	0 0 0 0	0 0 0 1	0 1 0 1
U2A, U2D	0 0 0 1	0 0 0 0	0 0 0 1	0 1 1 0

NOTE: Data Lines 0-7 = AD0-AD7
Data Lines 8-15 = A8-A15

U7 is enabled and a Y output goes low during the time that the $\overline{RD}$ or $\overline{WR}$ signal is low. If the $\overline{RD}$ signal enables U7, the addressed device is a tri-state buffer (paragraphs 1.7.2.6.1 through 1.7.2.6.3) which is enabled by the low pulse from a U7 output; however, if the $\overline{WR}$ signal enables U7, the resultant high-to-low level from U7 to the clock input of the addressed device does not change the status of the device. After the microprocessor replaces the address on the bus with data, the $\overline{WR}$ line goes high and U7 is disabled. The U7 output that went low when the $\overline{WR}$ line was low now changes state; this positive-going clock transition latches the data into the addressed device (paragraph 1.7.2.5).

1.7.2.5 Write-Only Registers

Four registers, U3B, U10, U11, and U12, serve the microprocessor as write-only devices. Each register latches the data on its D inputs to the Q outputs on a positive-going transition of its clock pulse.

To initiate a write operation, the microprocessor places the address of the device on the data bus and issues the ALE signal, latching the lower-order bits of the address into U13. The processor pulls the $\overline{WR}$ line low and address decoder U7 is enabled (paragraph 1.7.2.4.2). U7 decodes the address latched by U13, and the Y output connected to the clock or clock pulse input of the addressed device goes low. Y0 is the clock input to U3B and Y1, Y2, and Y3 are the clock pulse inputs to U10, U11, and U12, respectively.

Next, the processor pulls the $\overline{WR}$ line high, signaling that the data are on the bus. At this point, the high level on $\overline{WR}$ disables U7 and the Y output that was low, makes a positive transition; this positive-going pulse latches the data into the addressed device.

The functions of the four write-only registers are described in the paragraphs that follow.

1.7.2.5.1 Local/Remote Select (U3B)

Register U3B provides a select level to gain voltage switch U8B. The microprocessor reads the status of the front panel tuning disable switch (during a read operation on the Synthesizer Interface Board (232-A1)) to determine if the receiver is in the local or remote operating mode. The local/remote status is contained in the LSB of the local/remote data byte. The bit is low if the receiver is in local mode and high if the receiver is in remote mode. The logic level is applied to the D input of the flip-flop U3B, via data line AD0. The bit level is latched to the Q output of U3B when the clock input makes a positive transition. From U3B, the pulse representing the local/remote code is applied to the select input of U8B (paragraph 1.7.2.9.1). U8B switches between manual and remote RF gain voltage.

1.7.2.5.2 Bandwidth and BFO Inhibit (U10)

Table 1-30 shows the data word for U10. The microprocessor writes data into register U10 when a bandwidth parameter is changed or updated (every cycle), remotely or locally, and when the BFO is to be activated or deactivated. The Q0 through Q6 outputs of U10 connect through 232-XA2B to the bandwidth circuits in the IF section of the receiver; a high logic level on one of the bandwidth lines indicates selection of that bandwidth. The Q7 output is the BFO inhibit signal to the BFO Synthesizer (A5A3); a high logic level on this line disables the BFO.

Table 1-30. Address 1011 (U10) Data Word	
Output	Function
Q7	BFO Inhibit
Q6	16 kHz (A) IF Bandwidth
Q5	Optional
Q4	16 kHz (B) IF Bandwidth
Q3	6 kHz IF Bandwidth
Q2	3.2 kHz IF Bandwidth
Q1	1.0 kHz IF Bandwidth
Q0	0.3 kHz IF Bandwidth

1.7.2.5.3 Gain/Detection Mode (U11)

Table 1-31 is the data word for U11. The microprocessor updates receiver gain and detection mode parameters by writing the data into register U11. The Q outputs connect through 232-XA2B to the detection mode and AGC circuits in the IF section of the receiver. A high logic level indicates the selected gain or detection mode; the high level activates the IF circuit to initiate the parameter change.

The manual gain line from output Q6 is also applied to the select input of RF gain voltage switch U8A and B, discussed in paragraph 1.7.2.9.1. The ISB line from output Q3 is also applied to the select input of audio switch U8C, described in paragraph 1.7.2.9.2.

1.7.2.5.4 Remote RF Gain (U12)

Remote RF gain is received as an 8-bit binary coded word and is written to the inputs of register U12 by the microprocessor. U12 is addressed for a write operation only when the receiver is in remote operating mode. The RF gain code is from 111111 (minimum gain) to 000000 (maximum gain). The Q outputs of U12 connect the binary RF gain word to digital-to-analog (D/A) converter U20, described in paragraph 1.7.2.7.1; this D/A converter generates the RF gain voltage, between zero and five volts.

Table 1-31. Address 1012 (U11) Data Word	
Output	Function
Q7	SLOW AGC
Q6	MAN AGC
Q5	LSB
Q4	ISB
Q3	USB
Q2	CW
Q1	FM
Q0	AM

1.7.2.6 Read-Only Devices

1.7.2.6.1 Gain and Detection Mode Gates (U2B, D)

U2B and D are two of four tri-state buffer gates contained in the U2 integrated circuit. The gates are enabled (output equals input) by a low logic level on the enable inputs. The enable input to each gate is provided by the Y6 output of address decoder U7 (paragraph 1.7.2.4). When enabled, the output of each gate is connected to the ground point on the input to the gates.

The gates are enabled when the microprocessor initiates a read operation at address 1016. The data bus is tri-stated by the microprocessor and the bus lines, connected to the front panel detection and gain mode switches, reflect the status of the switches. The enabled gates (U2B and D) provide a ground return causing a closed switch to be indicated by a low logic level on the associated data bus line. Table 1-32 lists the corresponding functions of the data bus when the microprocessor reads the status of the front panel mode switches.

Table 1-32. Address 1016 (U2B, D) Data Word

Bit	Function
AD7	SLOW AGC
AD6	MAN AGC
AD5	LSB
AD4	USB
AD3	ISB
AD2	CW
AD1	FM
AD0	AM

1.7.2.6.2 Bandwidth and Zero BFO Gates (U2A, C)

U2A and C are two of the gates contained in quadruple gate tri-state buffer U2 and function identically to the gates described in paragraph 1.7.2.6.1. The configuration of the gates is such that when a low logic level is applied to the enable inputs from the Y5 output of address decoder U7 (paragraph 1.7.2.4), the output of the gates will equal the inputs.

U2C provides a common return for a closed front panel bandwidth switch, which appears on the associated bus line as a logic low, and U2A allows the AD7 bus line to indicate when the zero BFO switch is closed. The gates are enabled, allowing the microprocessor to monitor the status of the front panel bandwidth and zero BFO switches, when a read operation is initiated at address 1015. Table 1-33 lists the functions of the data bus lines.

Table 1-33. Address 1015 (U2A, C) Data Word	
Bit	Function
AD7	Zero BFO
AD6	Not Used
AD5	Optional
AD4	16 kHz IF Bandwidth
AD3	6 kHz IF Bandwidth
AD2	3.2 kHz IF Bandwidth
AD1	1.0 kHz IF Bandwidth
AD0	0.3 kHz IF Bandwidth

1.7.2.6.3 Signal Strength Gate (U14)

Octal tri-state buffer U14 drives the eight lower-order data bus lines, AD0 through AD7, when enabled by a low logic level from the Y4 output of address decoder U7 (paragraph 1.7.2.4). The enable input is provided when the microprocessor initiates a read operation at address 1014. The data on the bus when U14 drives the lines are the bits of the binary coded signal strength word output of A/D converter U20, discussed in paragraph 1.7.2.7.1. The U14 signal strength data word range is between binary 000000, representing no signal, and 111111, representing maximum signal strength.

1.7.2.7 Signal Strength Network

The signal strength voltage from the AGC circuits in the receiver enters the IF Interface Board through 232-XA2B and is applied to the non-inverting input of unity gain amplifier U18A. The output of U18A is applied to the front panel SIG/AUD meter through J1 and is applied to the analog-to digital converter U20 to be converted to binary form, allowing the microprocessor to monitor the signal strength.

1.7.2.7.1 Signal Strength Conversion (U20)

The analog-to-digital converter, U20, contains a network of 256 resistors (each 300 ohms) in series. Analog switch taps are made at the junction of each resistor and at each end of the network. In operation, a reference voltage, provided by the external voltage divider formed by R9, R10 (adjustable for tuning the voltage), and R22, is applied across the 256 resistor network. The analog input (signal strength voltage) is applied through amplifier U18B and amplitude limiter VR4, to pin 12 of U20, and is compared to the center point of the internal ladder via the appropriate internal switch. If the analog voltage (V IN) is greater than one-half of the reference voltage (V REF), the internal logic changes the switch points and compares V IN and 3/4 V REF. This process, known as successive approximation, continues until the best match of V IN and V REF/N is made; N defines a specific tap on the resistor network (internal). When the conversion is complete, the logic loads a binary word corresponding to this tap (N)

into the output latch, where the valid data are held until a new conversion is completed and new data are loaded into the latches. The data transfer occurs in about 200 nanoseconds, so that valid data are present virtually all of the time. The binary coded output of the converter is the input to inverting tri-state buffer U14, read by the microprocessor to monitor the signal strength.

1.7.2.8 RF Gain Conversion (U19)

The 8-bit binary coded RF gain (remote) word from register U12 (paragraph 1.7.2.5.4) is applied to the A1 through A8 inputs of digital-to-analog (D/A) converter U19. The converter provides an output current directly related to the coded RF gain word. The current, from zero to two milliamps, is converted to voltage across the U17B feedback resistor, R15. This remote RF gain voltage is switched with locally selected RF gain voltage by U8B, discussed in paragraph 1.7.2.9.1.

The D/A converter consists of a reference current amplifier, an R-2R ladder (paragraph 1.7.2.8.1), and eight high-speed current switches (transistors). The switches are non-inverting; therefore, a high state on an input (A1 through A8) turns on the specified output current. The R-2R ladder divides the reference amplifier into binary-related components, which are fed to the switches. The reference amplifier (internal) is activated by the voltage (V REF+) at pin 14, provided by the VR1 and R14 current reference network. R14 is adjustable to fine tune the reference current.

External resistor R12 provides temperature stability. C16 is used to maintain a proper phase margin.

The general operating characteristics of an R-2R ladder are discussed in the following paragraph.

1.7.2.8.1 R-2R Ladder Theory

Figure 1-14 is an equivalent circuit for a 2-bit R-2R ladder; the table lists the voltage ratios. There are two general properties of an R-2R ladder:

1. The resistance looking back toward the Z or ground terminal of the ladder junction point is always equal to R.

2. For each step that a voltage has to be processed up the ladder toward X, its contribution is decreased by a factor of 2.

The U19 converter uses the above principles but the capacity of the ladder is increased to 8-bits. There is a remainder current which equals the LSD.

1.7.2.9 Multiplexer U8

Integrated circuit U8 is a triple two-channel multiplexer having three separate digital control inputs (A, B, and C) and an inhibit input. Each control input operates one of a pair of channels which are connected in a single-pole double-throw configuration.

The U8 inhibit input at pin 6 is tied to ground, holding the multiplexer in an enabled condition.

V_B	V_A	V_X
0	0	0
0	V	$\frac{V}{4}$
V	0	$\frac{V}{2}$
V	V	$\frac{3V}{4}$

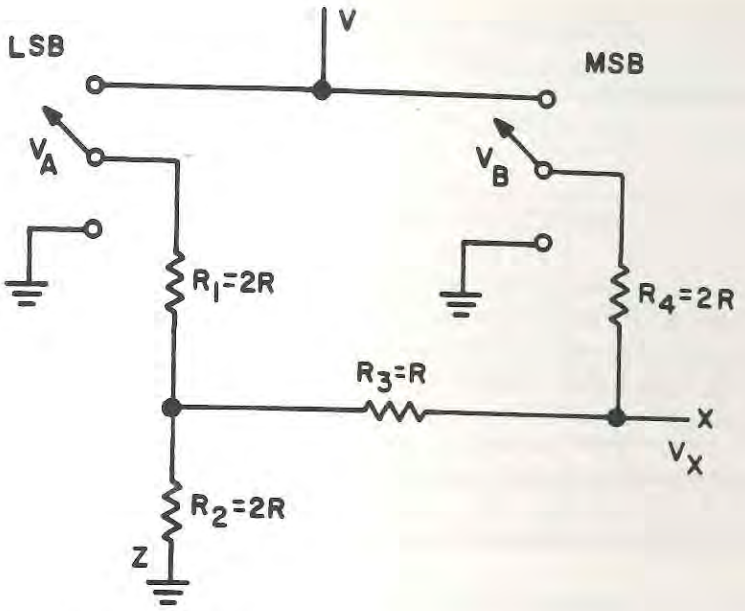


Figure 1-14. 2-Bit R-2R Ladder

1.7.2.9.1 RF Gain Voltage Switch (U8A, B)

Switches U8A and U8B switch the manual and remote RF gain voltages. The manual RF gain voltage is applied to the X0 input of U8B and the remote RF gain voltage is applied to X1. The X0 input is connected to the X output if the level at the A input is low; the X1 input is connected to the X output if the A input level is high. The A input level is dependent on the remote/local bit from U3B (paragraph 1.7.2.5.1). If the receiver is in remote mode, the bit is high and remote RF gain voltage is selected; in local mode, the bit is low and manual RF gain voltage is selected.

The selected RF gain voltage is applied to the Y1 input of U8A and is connected to the Y output when the level at the B input goes high. The B input is high when the selected gain mode is MAN AGC.

1.7.2.9.2 Audio Switch (U8C)

In any detection mode but ISB, the audios on the ring and tip of the front panel stereo phone jack are the same; in ISB detection mode, U8C switches the audio so that the USB audio is on the tip of the jack and LSB audio is on the ring, allowing both audios to be monitored with a 600 ohm stereo headphone.

The logic level at the input to U8C selects which audio is output at Z; this is the audio that goes to the ring of the phone jack. The C input is the ISB bit of the detection mode word output of U11. The bit is high only when ISB has been selected, remotely or locally. Operation of the switch is as follows.

The ISB/LSB audio from the IF section of the receiver is coupled to the Z1 input of U8C across C24 and the voltage divider formed by R29 and R30. C4 blocks the dc element of the audio signal and the voltage divider biases the signal at 2.5 volts above ground. In the ISB detection mode (C = 1), this audio signal (ISB/USB) is connected to the Z output of U8C.

In all other detection modes (C = 0), the Z0 input is connected to the Z output. The Z0 signal is the combined audio. Diodes CR7 and CR8 are protection diodes, provided because the combined audio level can exceed the voltage limits of U8C. C23 blocks the dc level of the combined audio signal, and the voltage divider formed by R27 and R28 biases the signal at +2.5 Vdc.

1.7.3 ASYNCHRONOUS I/O BOARD (232-A3)

The Asynchronous I/O Board interfaces the microprocessor in the receiver's control block with the remote control equipment. The WJ-8718/232 Option block diagram, Figure 1-5, illustrates the relationship between the microprocessor and the I/O board. Figure 1-24 is the 232-A3 schematic diagram.

The majority of board components are powered by +5 Vdc, applied across bypass capacitors C1, C6, C7, and C8. The zener voltage reference circuit, formed by VR1, VR2, R1, R2, and C2 through C5, provides potentials of +12 and -12 Vdc for the U7 and U8 logic gates and +12 Vdc for the baud rate generator, U5.

1.7.3.1 Address Latch (U2)

Integrated circuit U2 is an octal D-Type flip-flop. The clear (CLR) input is held high by Vcc, causing information at the D inputs to be latched to the Q outputs on the positive-going edge of the clock pulse. The clock pulse to U2 is the microprocessor control line ALE, inverted by U6C. ALE goes low, (and is inverted) when a valid address has been placed on the data bus. The resultant positive-going clock pulse to U2 latches the lower-order address bits to the Q outputs (Q6 and Q7 are unused). From the outputs of U2, five of the address bits are decoded as necessary to clock or enable the two addressable circuits on the I/O board: U1, discussed in paragraph 1.7.3.8, and U3, discussed in paragraph 1.7.3.4. The LSB of the address is described in paragraph 1.7.3.8.5.

1.7.3.2 Address Decoder U4

U4 is a three-to-eight line decoder, enabled by one high and two low logic levels on the G inputs, as shown in Table 1-34. When U4 is enabled, the three select inputs at A, B, and C are decoded and one of the eight outputs goes low. In this WJ-8718/232 Option application, only two outputs, Y0 and Y1, are used.

Table 1-34. U4 Truth Table

Inputs						Outputs	
Enable			Select				
G1	G2A	G2B	A	B	C	Y0	Y1
H	L	L	L	L	L	L	H
H	L	L	L	L	H	H	L

1.7.3.2.1 Decoder Enable

The G1 enable input to U4 is the bit that is carried on the A12 data line. Table 1-35 lists the addressable devices on the I/O board. The A12 bit is high when the MSD of the hexadecimal address is 1 (0001). G2B is the inverted (by U6A) level of the AD5 address bit.

To provide the two low levels to enable U4, AD5 must be high and AD4 must be low. As shown in Table 1-35, the enabling conditions exist when one of the hexadecimal addresses 1020, 1021, or 1022 has been placed on the data bus.

Table 1-35. Addresses 1020, 1021, and 1022

Address Bit	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0	2^3 2^2 2^1 2^0
Data Line	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	0 0 0 0
U1	0 0 0 1	0 0 0 0	0 0 1 0	0 0 0 1
U3	0 0 0 1	0 0 0 0	0 0 1 0	0 0 1 0

NOTE: Data Lines 0-7 = AD0 - AD7
Data Lines 8-15 = A8 - A15

1.7.3.2.2 U4 Select

The select inputs to U4 at A, B, and C are the address bits carried on the AD1, AD2, and AD3 data lines. (Note that the least significant bit of the address, carried on AD0 is not a decoder input. This bit has a unique use and is discussed in paragraph 1.7.3.8.5.)

Two of the eight available outputs of U4 are used to enable the two addressable devices (U1 and U3) on the I/O board. Comparison of Tables 1-34 and 1-35 shows that the Y0 output goes low when one of the two U1 addresses is latched by U2, and Y1 goes low when the U3 address is latched.

1.7.3.3 Switch Assembly (S2)

The eight-position switch assembly (S2) is used, prior to remote operation, to establish receiver address, for receiver master/slave configuration, and to enable parity check; if parity is enabled, the switch also establishes odd or even parity. Table 1-3 lists the switch functions. A high logic level indicates a closed switch and a low logic level indicates an open switch.

Paragraph 1.4.4, part of the preparation for operation procedure, contains a description of the switch settings.

1.7.3.4 Tri-State Buffer/Inverter (U3)

Octal tri-state buffer U3 allows the microprocessor to read the settings of the S2 switch assembly. The buffer inputs, to the microprocessor, the logic levels of the switch settings from the pull-up resistive network, U11. The outputs of U3 are tri-stated if the logic levels at the enable inputs (pins 1 and 19) are high. When the enable inputs go low, the outputs of U3 are taken out of tri-state and the data from the S2 switch assembly are inverted and placed on the lower-order address/data bus lines. U3 is enabled when the $\overline{RD}$ signal from the microprocessor goes low (after the address is latched) and when U4Y1 is low. As discussed in paragraph 1.7.3.2.2, U4Y1 is low only when address 1022 is latched by U2.

The microprocessor initiates a read operation to address 1022 (U3) to determine if the equipment address on incoming data is valid.

1.7.3.5 Baud Rate Network (U5, S1)

Baud rate is established by entering a baud rate select code in the four-position switch assembly, S1, described in paragraph 1.4.1. Baud rate generator U5 is an N-Channel LSI device capable of generating 16 selected frequencies (Table 1-2) from a single input frequency.

The baud rate generator is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to 2 less 1 (32,767). The device is driven by external crystal Y1 with a resonating frequency of 5.0688 MHz. Pin functions are listed in Table 1-36.

Table 1-36. Baud Rate Generator Pin Functions

Pin No.	Symbol	Name	Function
1	X1	Crystal input 1	One pin of Y1
2	X2	Crystal input 2	One pin of Y1
3	VCC	Power supply	+5 Vdc
5	GND	Ground	Common return
8	FO	Reference frequency	Reference output at 1/4 F IN
9	ST	Strobe	A high logic level loads inputs A, B, C, and D into U5.
10-13	A,B,C,D	Input address	Logic levels select F OUT.
14	F OUT	Output frequency	Frequency selected by input address

1.7.3.6 Active Repeater Network

The J1 and J2 connections on the I/O board allow up to 32 receivers to be "daisy-chained" and placed under control of one RS-232 Bus compatible controller. J1 connects to the rear panel REMOTE INPUT and J2 connects to the rear panel MONITOR OUTPUT. In the "daisy-chained" configuration, the monitor output of a receiver is connected to the REMOTE INPUT of the next receiver in the chain (Figure 1-3); the remote control equipment connects to the REMOTE INPUT of the first receiver in the chain.

Signal and data transmissions are applied to each unit in the chain and are accepted by the addressed unit or units; each I/O board actively repeats the transmissions (in both directions), assuring signal integrity.

Each handshake signal (RTS, DTR, DSR, and CTS) and each data bit (Rx and Tx data) passes through a repeater network consisting of a gating circuit and an inverter. The function of each line and the repeater network logic is discussed in the description of USART U1.

1.7.3.7 SYNC TxC/RxC Signals

The Asynchronous I/O Board is wired (Figure 1-24) for asynchronous operation with baud rate established in switch assembly S1 and generated by U5 (paragraph 1.7.3.5). The SYNC TxC and RxC signals are for synchronous operation, with baud rate established by the controller. Alternate connections at J11 and J14 allow application of the synchronous signals to the USART; however, program memory devices in the WJ-8718/232 Option must be returned to Watkins-Johnson, Gaithersburg, Maryland for re-programming if synchronous operation is desired.

1.7.3.8 Universal Synchronous/Asynchronous Receiver/Transmitter (USART, U1)

The USART (U1) is a peripheral device designed for data communications. The USART receives and transmits data between the microprocessor on the IF Interface Board and external control equipment. The functional format of the USART is programmed by the microprocessor prior to data transmission.

Internal to the USART, an 8-bit data bus coordinates the exchange of data between buffers, logic, and control circuits in response to control and handshake signals applied to the USART by external devices. Basically, the USART provides two services in response to the externally applied signals: it converts parallel data from the microprocessor to a serial data stream and transmits this stream to the remote controller; or, it receives a serial stream of data from the controller, converts the data to parallel format, and transmits the data to the microprocessor. The USART generates signals which inform the microprocessor and the controller when it is ready to transmit or receive; the signals ensure the orderly transfer of data. Data are transmitted from the USART on the TxD line and received by the USART on the RxD line (paragraphs 1.7.3.8.14 and 1.7.3.8.15).

The activities of the USART are timed by the CLK, $\overline{\text{RxC}}$, and $\overline{\text{TxC}}$ inputs, and regulated by the logic levels on the control input lines (RST $\overline{\text{IN}}$, $\overline{\text{CS}}$, $\overline{\text{C/D}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) and the handshake input lines ($\overline{\text{CTS}}$ and $\overline{\text{DSR}}$). The signals generated by the USART are Rx RDY and Tx RDY, to the microprocessor, and $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$, to the remote controller. The input and output signals are described in paragraphs 1.7.3.8.1 through 1.7.3.8.15.

1.7.3.8.1 RESET Signal

A high logic level on the RST $\overline{\text{IN}}$ line resets the internal circuits of the USART. The RST $\overline{\text{IN}}$ signal is generated by the microprocessor when power is applied. Following reset, before data transmission can begin, the USART must be programmed by the microprocessor. The programming procedure establishes general operating characteristics of the USART and must follow each USART reset.

1.7.3.8.2 Clock Input

The Clock (CLK) input is provided to establish the time base for internal activities of the USART. Clock rate is established by the baud rate generator, U5.

1.7.3.8.3 Receiver Clock/Transmitter Clock

The Receiver Clock ($\overline{\text{RxC}}$) and the Transmitter Clock ($\overline{\text{TxC}}$) establish the rate of data transmission. Characters are shifted out of the USART on the falling edge of $\overline{\text{TxC}}$; input data are sampled on the rising edge of $\overline{\text{RxC}}$. The rate of the two clock signals is established by

coded entries to the S1 switch assembly (paragraph 1.7.3.6). The 16 selectable rates are between 50 and 19,200 baud. $\overline{RxC}$ and $\overline{TxC}$ are 16 times the baud rate.

1.7.3.8.4 Chip Enable Input ($\overline{CS}$)

The $\overline{CS}$ signal must go low to enable the USART. The signal is generated by decoder U4 (paragraph 1.7.3.2) when one of two USART addresses has been placed on the bus by the microprocessor and latched by U2 (paragraph 1.7.3.1). The two addresses, hexadecimal 1020 and 1021, differ only in the logic level of the LSB, which determines the level of the C/$\overline{D}$ signal, described in the following paragraph.

1.7.3.8.5 Control/Data Signal (C/$\overline{D}$)

The C/$\overline{D}$ line is logic high when the USART address 1021 is used. The microprocessor uses this address to indicate to the USART that the data to follow are mode or command instructions. Following a USART reset, the first control word the microprocessor must issue is a mode instruction which defines the general operating characteristics of the USART. The second control word is a command instruction which defines a status word used to control the operation of the USART.

The USART address 1020 places a logic low level on the C/$\overline{D}$ line, and is used by the microprocessor to inform the USART that a read or write data transmission is to follow.

1.7.3.8.6 Read/Write Signals ($\overline{RD}$/$\overline{WR}$)

A $\overline{RD}$ or $\overline{WR}$ signal is pulled low by the microprocessor when a read or write operation is to be initiated at the addressed device. The $\overline{RD}$ and $\overline{WR}$ signals have no effect on the USART unless the $\overline{CS}$ (enable) signal is low. Refer to paragraph 1.6.5.4 and Figures 1-7 and 1-8 for information concerning read and write operations.

1.7.3.8.7 Data Input/Output Lines

The D0 through D7 input/output ports of U1 are connected to the lower-order address/data lines on the microprocessor data bus. Data are loaded on the bus by the microprocessor and enter the D ports of U1 during a write operation. During a read operation, data are loaded on the bus from the D ports of the USART.

1.7.3.8.8 Receiver Ready (Rx RDY)

The Rx RDY signal, generated by the USART, goes high to inform the microprocessor that an entire character has been received from the remote controller and is ready to be fetched by the microprocessor. The microprocessor treats the Rx RDY signal as an interrupt request, halts its main program, and branches to a subroutine to execute the instructions there. During the course of these instructions, the data in the USART are read and the Rx RDY automatically resets (goes low).

1.7.3.8.9 Transmitter Ready (Tx RDY)

The Tx RDY signal is raised high by the USART to inform the microprocessor that the USART is ready to receive data from the microprocessor. The microprocessor interprets

the Tx RDY signal as an interrupt request, branches from the main program to a subroutine, and executes the subroutine instructions. The Tx RDY signal automatically resets (goes low) when the microprocessor writes data into the USART. Data written into the USART are automatically transmitted via the USART as long as $\overline{CTS}$ is active (low).

1.7.3.8.10 Data Set Ready ($\overline{DSR}$)

The $\overline{DSR}$ signal into the USART goes low when the remote controller is ready to send data. The signal is applied to an active repeater network in each receiver under control. Figure 1-15 illustrates the flow of a signal ($\overline{DSR}$ or $\overline{CTS}$) from the control equipment through circuits representative of the repeater networks in three receivers. Additional receivers (up to 32) could be connected to the receiver chain in the manner depicted in the illustration. The logic levels illustrated are typical of an activated $\overline{DSR}$ signal; the opposite logic levels are the steady state condition.

1.7.3.8.11 Data Terminal Ready ($\overline{DTR}$)

The $\overline{DTR}$ line from the USART goes low to inform the remote controller that the USART is ready to receive. This signal will go low only from the addressed receiver (or receivers, if more than one receiver has the same address) and will be actively repeated by the I/O boards in the receivers along the path to the controller. Figure 1-15 illustrates a typical network of one controller and three receivers under control. The control signal into the controller represents the $\overline{DTR}$ (or $\overline{RTS}$) signal. Circuits shown are equivalent to the repeater networks. In the figure, the logic levels on the receiver-to-controller lines are steady-state conditions.

1.7.3.8.12 Clear to Send ($\overline{CTS}$)

A low logic level on the $\overline{CTS}$ input to U1 tells the USART's that the controller is ready to receive a transmission from the USART. The signal reaches the USART's through circuits identical to the $\overline{DSR}$ signal path, described in paragraph 1.7.3.8.10. The USART will not transmit data unless $\overline{CTS}$ is active (low).

1.7.3.8.13 Request to Send ($\overline{RTS}$)

A low logic level on the $\overline{RTS}$ output from the USART notifies the controller that the USART is now ready to transmit. The signal reaches the controller through circuits identical to the circuits discussed in the $\overline{DTR}$ signal description in paragraph 1.7.3.8.11.

1.7.3.8.14 Received Data (RxD)

The serial data stream on the RxD input to the USART contains the instructions from the remote control equipment. The data word is an 11-bit character consisting of a start bit, parity bit (if parity is enabled), eight data bits, and a stop bit. Data format is discussed in paragraph 1.5.2. Figure 1-16 illustrates a remote controller with three receivers under control. Circuits equivalent to the repeater networks in the receiver illustrate the flow of receive and transmit data through the receivers. The logic levels are based on the assumption that receiver 3 is the addressed unit. Logic gates in the repeater network invert the logic sense of received data between the USART and the RS-232-C bus. The gates also switch signal levels between TTL and 232 logic.

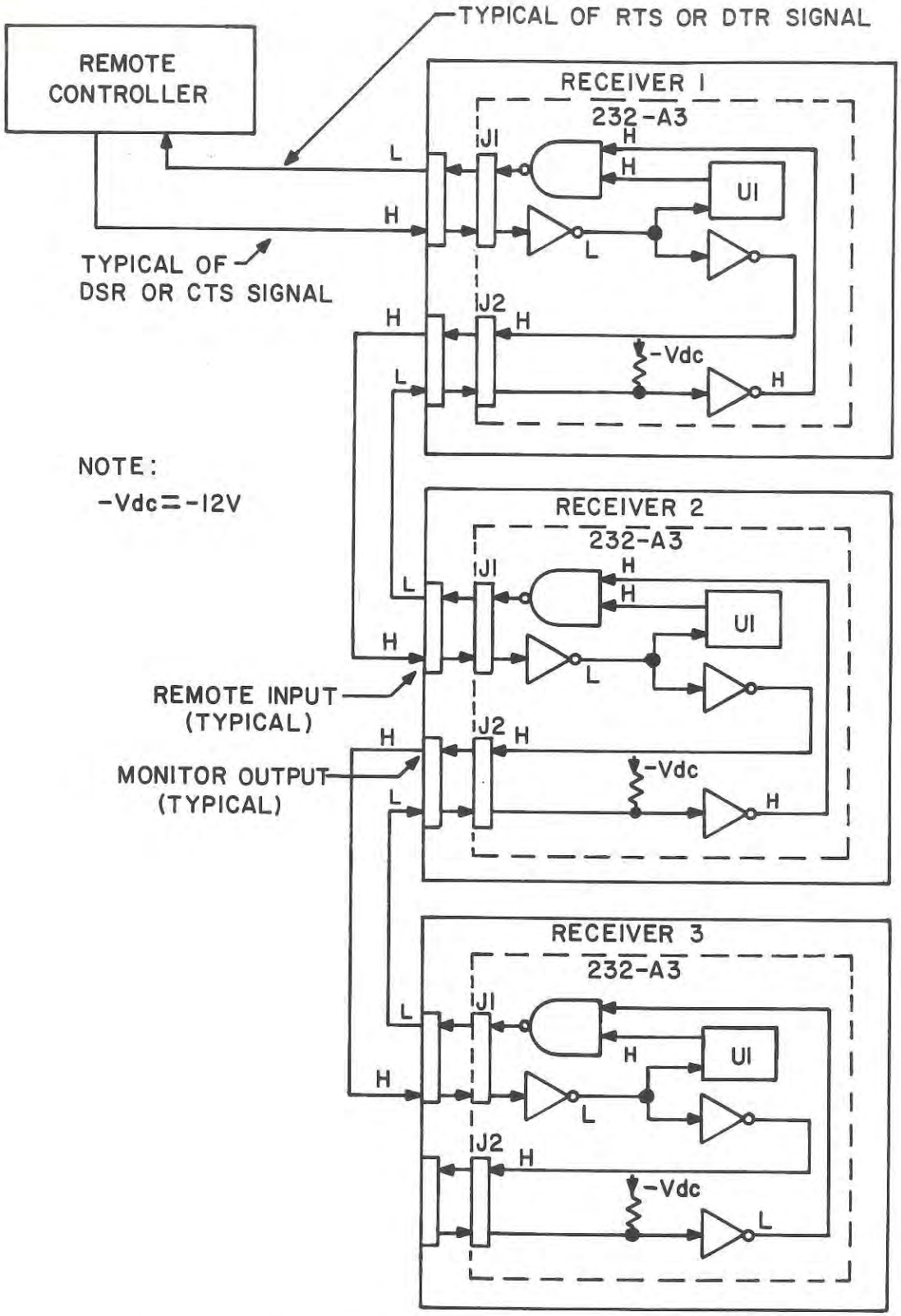


Figure 1-15. Equivalent Circuits for Handshake Signals

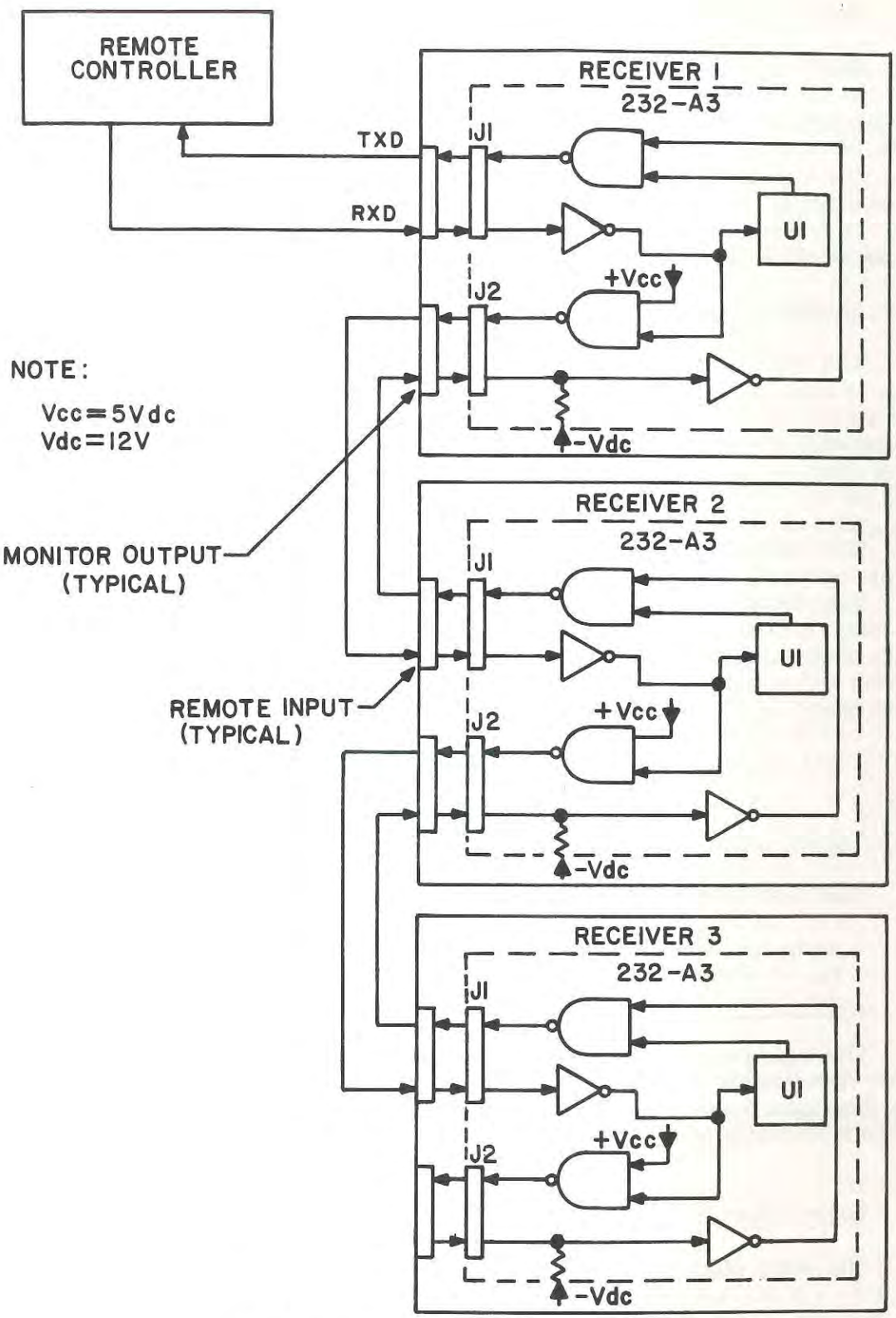


Figure 1-16. Equivalent Circuits for RxD and TxD Signals

1.7.3.8.15 Transmitted Data (TxD)

The information on the TxD line is a serial data stream transmitted from the USART to the remote control equipment. The data are the current receiver parameters as requested by the controller. See paragraph 1.5.2 for information about data format. Figure 1-16 illustrates the flow of transmit data through a controlled network of three receivers. The circuits in the illustration are representative of the repeater network which assures the integrity of the data signals. The logic gates in the repeater network invert the logic sense of transmitted data between the USART and the RS-232-C bus. The gates also switch signal levels between TTL and 232 logic.

1.8 MAINTENANCE

The maintenance procedures in Section IV of the WJ-8718 HF Receiver Instruction Manual can be adapted and applied to a receiver equipped with the WJ-8718/232 Option. The procedures should be supplemented with the information contained in paragraphs 1.8.1 through 1.8.4.2 of this WJ-8718/232 Option Instruction Manual; all references to the Type 791828 Front Panel Interconnect and the Type 791575 Manual Up/Down Counter Boards should be considered void.

1.8.1 TEST EQUIPMENT

The WJ-8718/232 Option contains a large number of digital integrated circuits (IC's). The most efficient method of testing and troubleshooting digital IC's, in most cases, is to use a Logic Troubleshooting Kit containing probes capable of supplying and detecting digital voltage levels and pulses. A typical set of probes, the Hewlett-Packard 5022A Multi-Family Logic Troubleshooting Kit, is recommended. This kit contains the following devices:

545A	Logic Probe
546A	Logic Pulser
547A	Current Tracer
548A	Logic Clip

The basic functions of these devices are described in paragraphs 1.8.1.1 through 1.8.1.4.

1.8.1.1 Logic Probe

The logic probe detects logic levels and pulses without the need for a voltmeter or oscilloscope. The lamp in the probe tip shows a bright light for a logic high, no light for a logic low, and a dim light for a floating or bad logic level. When a pulse train of up to 50 MHz is detected, the lamp blinks at a rate of 10 Hz. Power for the probe is supplied by the unit under test.

1.8.1.2 Logic Pulser

The logic pulser probe provides pulses that are compatible with digital circuits. When the probe tip is placed against a circuit point, the probe senses the logic level present, and when the pulse button is pressed, the circuit is briefly pulsed to the opposite state. By using the logic probe and logic pulser in combination, a known input can be supplied to an IC, and the effect can be observed at the output.

1.8.1.3 Current Tracer

The current tracer probe senses the magnetic field produced by current flow in the circuit. It can be used to trace current from the source to the sink; therefore, it can be helpful in finding short-circuits, or in determining if an IC output is actually sourcing current, and, if so, in finding out where the current is flowing.

1.8.1.4 Logic Clip

The logic clip indicator displays the logic level present at all of the terminals of an IC at the same time. The readout is 16 LED's that glow if the terminal is high and are dark if the terminal is low. When used in combination with the logic pulser, the effect of input pulses on all of the terminals of the IC under test can be observed.

1.8.2 PERFORMANCE TESTS

Performance tests should be utilized to confirm operating specifications during initial inspection, during periodic checks, or after repairs have been made. A receiver equipped with the WJ-8718/232 Option can be tested, in the manual operating mode, using the procedures as outlined in the WJ-8718 HF Receiver Instruction Manual. In the remote operating mode, the following guidelines should supplement each test procedure. It is assumed that the proper remote control equipment has been connected to the receiver under test and that the receiver has been prepared for operation per instructions in paragraph 1.4 of this supplement.

1. Energize the receiver under test and depress the front panel TUNING DISABLE button.

2. Use remote control command instructions (paragraph 1.5.2) to establish the receiver parameters listed in step 1 of the test procedure.

3. Proceed to carry out the test procedure instructions, using remote commands to change the receiver parameters as required during the test. If test results are satisfactory, the receiver is responding properly to the remote commands. If a problem becomes evident during a performance test procedure, refer to the troubleshooting section of the WJ-8718 HF Receiver Instruction Manual and to paragraph 1.8.4 of this supplement.

4. Initiate both full- and partial-status monitor operations and verify that the monitored data correspond to the most recently commanded parameters.

NOTE

When the receiver under test is in any sideband mode (ISB, LSB, or USB) the receiver will automatically be forced into the 16 kHz bandwidth.

5. Verify that the receiver status can be monitored with the front panel TUNING DISABLE pushbutton dis-engaged.

1.8.3 ALIGNMENT PROCEDURES

1.8.3.1 Alignment of Remote RF Gain

The RF gain of a receiver can be remotely controlled only when the TUNING DISABLE button is depressed and the receiver is in the manual gain mode. The RF gain voltage is aligned by changing the resistance of variable potentiometer 232-A2R14. Refer to Figures 1-20 and 1-23, location of components and schematic illustrations, to locate R14. Adjust R14, using the following procedure.

1. Energize the receiver under test and depress the TUNING DISABLE button.
2. Establish the manual gain mode and the minimum RF gain level, via remote command.
3. Attach an oscilloscope probe to pin B41 of 232-XA2B.
4. Adjust R14 until the oscilloscope measures a voltage of +5 Vdc.
5. Vary the RF gain by remote commands and verify that the voltage viewed at pin B41 of 232-XA2B decreases linearly to 0 Vdc as gain level is increased to maximum.

1.8.3.2 Alignment of Digitized Signal Strength

The digitized signal strength voltage is aligned by adjusting 232-A2R10. To locate the resistor, (R10) consult Figures 1-20 and 1-23, location of components and schematic diagrams. To align the voltage, use the following procedure.

1. Connect the test equipment as shown in Figure 1-17 and energize all equipment.
2. Tune the signal generator to provide a 15.005 MHz, CW signal at +10 dBm.
3. Establish the following receiver parameters, remotely or manually:

Detection Mode	CW
Bandwidth	16 kHz
Gain Mode	AGC FAST
Tuned Frequency	15.005 MHz

4. Connect the oscilloscope probe to each output pin of U20 and adjust R10 until all output levels are logic low.

NOTE

Because of inversion by U14, all bits of the monitored signal strength word should be logic high (maximum signal strength).

5. Decrease the drive from the signal generator in 10 dB decrements and verify that the monitored signal strength decreases in value.

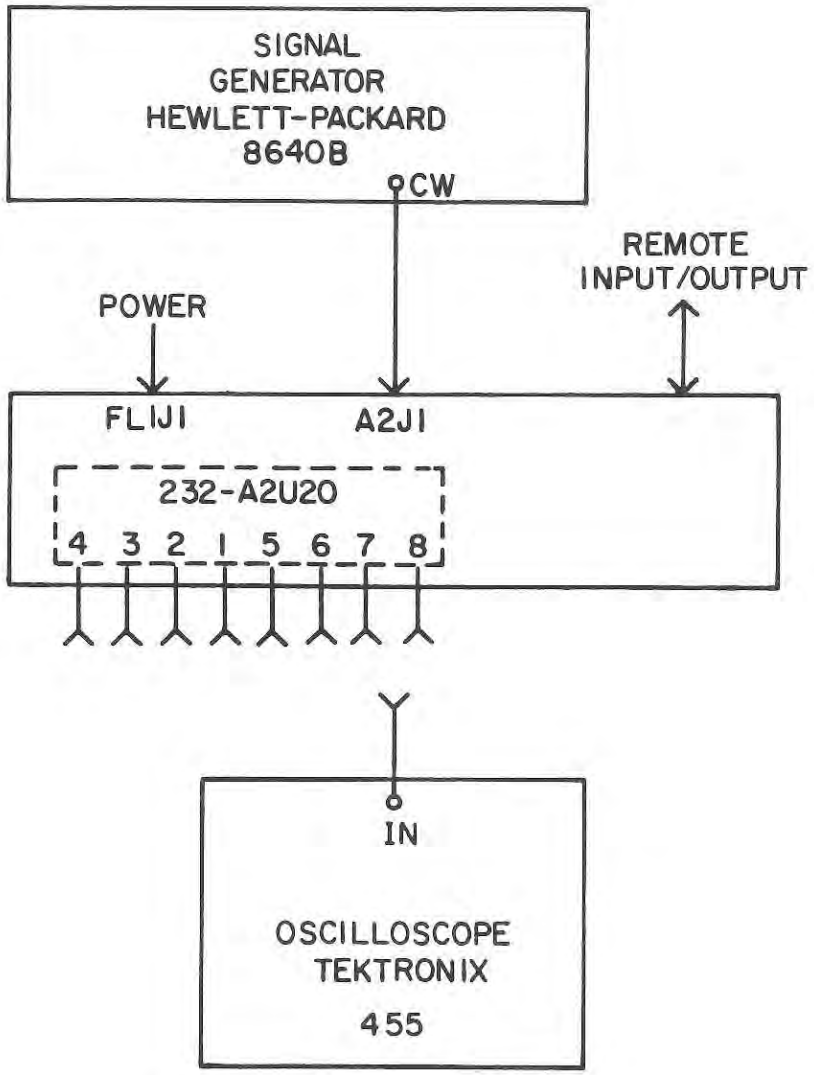


Figure 1-17. Signal Strength Alignment Equipment Setup

1.8.4 TROUBLESHOOTING

Figure 1-18, the WJ-8718/232 Option troubleshooting tree, will aid in isolating trouble in the digital circuits. General troubleshooting and repair information follows.

1.8.4.1 Symptoms of Integrated Circuit Failure

1. Open Input - The output of a digital IC that has an opened input (internal) will usually behave as if the input level as a static "high". The output of this IC will not respond to input pulses.

2. Opened Output - The output level of a digital IC that has an opened output (internal) will not respond to input pulses and will usually assume a "bad" level of approximately 1.5 volts. This "bad" level will often have the same effect as a "high" level on the input of the next IC in the circuit.

3. Short Circuit between Input and Ground or Vcc - If the input is shorted to ground, the device will react as through the input were "low". If the input is shorted to Vcc, the device will react as though the input were "high". Remember that either of these conditions can affect the output of the stage prior to this. A digital voltmeter (DVM) or oscilloscope can be used to distinguish between normal logic levels, and ground or Vcc. The logic pulser cannot override the Vcc or ground potential.

4. Short Circuit between Output and Ground or Vcc - As in the above cases, the output will not respond to pulses at the input. A DVM can be used to distinguish between normal logic levels and ground or Vcc.

5. Short Circuit between Two Inputs - This failure is not as easy to detect. The device will behave normally unless one input tries to go "high" while the other is "low". If this occurs, the short-circuit will hold both inputs low.

6. Internal Failure of Logic Circuits - The effect of this trouble is to lock the output in either the "high" or "low" state. The output will not respond to input pulses.

1.8.4.2 In-Circuit Tests

Digital IC's rarely have partial or intermittent failures; therefore, the failures may usually be located by simple static tests. The circuit troubleshooting procedure will normally isolate a failure down to the few IC's that could be involved in the circuit failure. The following series of steps will serve to locate most faulty IC's. A "node" is defined as a circuit branch common to one or more inputs and one or more outputs.

1. Refer to the appropriate data book(s) for the pin-out and diagram of the IC(s) under test.

2. Use the logic pulser to stimulate the inputs, while using the logic probe or logic clip to observe the response at the outputs. Make a note of each node that fails to respond to the stimulus, in the manner predicted by the truth table. The logic clip is especially useful for counters. (The term "node" is used to emphasize the fact that the failure of an IC to respond properly may be due to short-circuited tracks, or other failures external to the IC under test.)

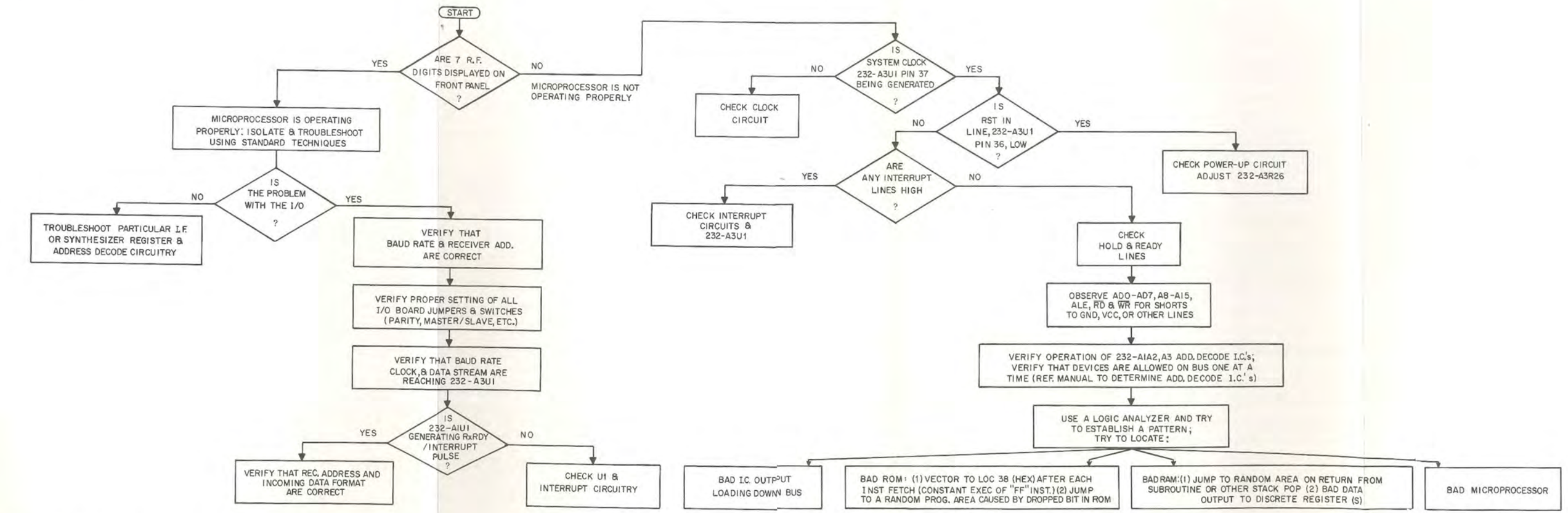


Figure 1-18. WJ-8718/232 Option Digital Troubleshooting Tree

NOTE

When an IC fails, it usually fails completely. Thus, it is not normally necessary to observe the timing of the output signals. If an IC performs correctly under static test, it can be assumed to be good.

3. When one or more failing nodes have been located, use the logic probe to check the output of the IC that is driving the node. The logic probe will indicate a "bad" level by showing a dim light. If a "bad" level is indicated, the IC driving the node should be replaced.

4. Check for a short circuit to ground or Vcc by placing both the logic probe and logic pulser on the terminal. The logic pulser can override normal TTL output levels, but cannot override power supply potentials. Therefore, the presence of a pulse indicates that the node is not short-circuited, and the absence of a pulse indicates the node is shorted to Vcc (if it is high) or to ground (if it is low). If a short circuit is indicated, proceed to step 5. If no short circuit to ground or Vcc is indicated, proceed to step 6.

5. A node short-circuited to ground or Vcc could be the result of either a short-circuited track on the board or an internal short in an IC. First, examine all branches of track connected to the node with the current tracer. Use the current tracer to isolate a defective IC; the circuit that draws the most current is generally defective.

6. If neither an open output (step 3), nor a node shorted to ground or Vcc (step 4) is indicated, look for a short between two nodes. This can be done more easily by turning OFF the unit's power, and using an ohmmeter to test for continuity between nodes that should not be common. (Refer to the schematic diagram.) If a short circuit between nodes is indicated, proceed to step 7. If a short circuit is not evident, proceed to step 8.

7. The most probable cause of a short circuit between two nodes is a solder bridge on the board. If the two nodes which are short-circuited are connected to the same IC, the short circuit might be internal to the IC. If no external short-circuit can be found, replace the common IC.

8. When open outputs and short circuits have been eliminated, the problem could be an open input on the IC being driven from the node, an internal IC failure, or an open signal path. The current tracer, or an ohmmeter, can be useful in finding an open signal path. For an opened input or an internal failure, the IC must be replaced.

1.8.5 REPAIR

1.8.5.1 General Repair Procedure

When a trouble has been isolated to a specific circuit board or assembly, the user may decide to make the repair himself or return the board or assembly to the factory for replacement or repair. After a repair has been made, alignment should be carried out, if necessary, and appropriate tests should be performed to verify proper operation.

1.8.5.2 Removing/Replacing Printed Circuit Components

Be careful not to damage the track when removing components from a printed circuit board. The soldering iron power should be no more than 40 watts, and a solder sipper or wicking procedure should be employed when removing solder. Non-corrosive soldering flux should be used when removing solder by wicking.

Removal of transistors which are soldered into printed circuit boards should be done with extra care. If the soldering iron is left on the wire lead of a transistor, heat travels up the wire and deforms the junction to which it is connected, destroying the transistor. To help prevent this, the transistor wire lead should be gripped, with a copper heat-sink or clamp, between the soldered joint and the transistor so that heat travelling up the wire will be transferred to the clip rather than the transistor.

Care must be taken so that an electrostatic difference of potential does not build up between transistors in a circuit and the soldering iron. The difference of potential can be reduced by touching the iron tip to a grounded point on the equipment just before soldering to another point in the circuit. Never solder transistorized equipment while it is operating.

Some soldering irons have ac flowing in a hairpin-shaped tip. The magnetic field from this haripin can induce voltages into transistor circuits that can burn out transistors.

Power transistors may have their cases bolted to a heat sink metal, but they often require insulation between the case and heat sink. A thin piece of mica coated with special silicon grease to improve heat conduction through it may be used. A resistance check should always be made to make sure the case and heat sink are insulated from each other.

In returning components to the board, make sure that the holes are clear and be careful that the leads do not catch the edge of the track and lift it from the board. A good grade of resin core 60/40 solder should be used. Heat no longer than is necessary to achieve a good joint and use a heat sink where possible.

When replacing CMOS integrated circuits, use a low power soldering iron. To avoid static charge buildup, do not handle CMOS integrated circuits with the fingers.

1.9 REPLACEMENT PARTS LISTS

The following list of manufacturers, and parts lists are intended as a supplement to the WJ-8718 Instruction Manual, and are to be used in conjunction with the applicable sections of that manual.

Mfr. Code	Name and Address
01686	RCL Electronics, Inc. 195 McGregor Street Manchester, NH 03102
06776	Robinson Nugent Inc. 800 E. 8th Street P.O. Box 470 New Albany, IN
09215	Brush Develop. Co. Cleveland, OH
18677	Scanbe Mfg. Corporation 3445 Fletcher Avenue El Monto, CA 91731
34371	Harris Semiconductor Div. Harris-Intertype Corp. P.O. Box 1883 Melbourne, FL 32901
34649	Intel Corp. 3065 Bowers Avenue Santa Clara, CA 95051
53848	SMC Microsystems Corp. 35 Marcus Blvd. Hayspauge, NY 11787
75037	Minnesota Mining and Mfg., Co. Electro Products Division 3M Center St. Paul, MN 55101

1.10 WJ-8718/232 I/O OPTION

REF DESIG	DESCRIPTION		QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
232-A1	Synthesizer Interface Board		1	796029-1	14632	
232-A2	IF Interface Board		1	796032	14632	
232-A3	Asynchronous I/O Board		1	796037	14632	
232-J1	Plug Assembly	Part of W2	1	206653-1	00779	
232-J2	Receptacle Assembly	Part of W3	1	206646-1	00779	
232-MP1	Adapter Plate		2	180027-1	14632	
232-P1	Connector, Plug, Multipin	Part of W1	3	3332-0000	75037	
232-P2	Same as 232-P1	Part of W1				
232-P3	Same as 232-P1	Part of W1				
232-P4	Connector, Plug, Multipin	Part of W2	2	88475-4	00779	
232-P5	Same as 232-P4	Part of W3				
232-W1	Cable Assembly		1	280097-1	14632	
232-W2	Cable Assembly		1	380059-1	14632	
232-W3	Cable Assembly		1	380060-1	14632	

1.10.1 TYPE 796029-1 SYNTHESIZER INTERFACE BOARD REF DESIG PREFIX 232-A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
BT1	Battery: 2.4 V	1	41B901BD16G1	19209	
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	5	8131M100-651-104M	72982	
C2 Thru C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 2.2 µF, 20%, 10 V	2	196D226X0010JE3	56289	
C7	Same as C6				
CR1	Diode	1	5082-2800	28480	
J1	Not Used				
J2	Connector, Receptacle, Multipin	3	87567-4	00779	
J3	Same as J2				
J4	Same as J2				
R1	Resistor, Fixed, Composition: 10 kΩ, 5%, 1/4 W	3	RCR07G103JS	81349	01121
R2	Same as R1				
R3	Resistor, Fixed, Composition: 820 Ω, 5%, 1/4 W	1	RCR07G821JS	81349	01121
R4	Same as R1				
R5	Resistor, Fixed, Composition: 390 Ω, 5%, 1/4 W	1	RCR07G391JS	81349	01121
R6	Resistor, Fixed, Composition: 47 kΩ, 5%, 1/8 W	2	RCR05G473JS	81349	01121
R7	Same as R6				
U1	Integrated Circuit	2	MC14050BCP	04713	
U2	Same as U1				
U3	Integrated Circuit	1	SN74LS125N	01295	
U4	Integrated Circuit	1	SN74LS00N	01295	
U5	Integrated Circuit	1	SN74LS139N	01295	
U6	Integrated Circuit	2	SN74LS138N	01295	
U7	Integrated Circuit	1	SN74LS173N	01295	
U8	Integrated Circuit	7	SN74LS273N	01295	
U9	Integrated Circuit	2	HM1-6561B-9	34371	
U10	Same as U9				
U11	Not Used				
U12	Not Used				
U13	Same as U8				
U14 Thru U18	Same as U8				
U19	Integrated Circuit	1	DM81LS95N	27014	
U20	Integrated Circuit	1	SN74LS365N	01295	
U21	Resistor Network: 10 kΩ	3	764-1-R10K	73138	
U22	Same as U21				
U23	Same as U21				
U24	Same as U6				
U25	Not Used				

REF DESIG PREFIX 232-A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U26	Integrated Circuit	1	841034	14632	
XU8	Socket, IC	7	ICL-203-S6-G	06776	
XU9	Socket, IC	4	US-2-18-110-G-B	18677	
XU10 Thru XU12	Same as XU9				
XU13 Thru XU18	Same as XU8				
XU25	Socket, IC	2	US-2-24-110-G-B	18677	
XU26	Same as U25				

1.10.2 TYPE 796032 IF INTERFACE BOARD REF DESIG PREFIX 232-A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C1	Capacitor, Electrolytic, Tantalum: 47 µF, 20%, 20 V	3	196D476X0020PE4	56289	
C2	Same as C1				
C3	Same as C1				
C4	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	10	8131M100-651-104M	72982	
C5 Thru C10	Same as C4				
C11	Capacitor, Mica, Dipped: 20 pF, 5%, 500 V	2	CM04ED200J03	81349	72163
C12	Same as C11				
C13	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 100 V	6	8131M100-651-474M	72982	
C14	Same as C4				
C15	Capacitor, Mica, Dipped: 330 pF, 2%, 100 V	1	CM04FA331G03	81349	72163
C16	Capacitor, Mica, Dipped: 15 pF, 5%, 500 V	1	CM04CD150J03	81349	72163
C17	Same as C13				
C18	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	2	196D105X0035HE3	56289	
C19	Same as C18				
C20	Same as C4				
C21	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	2	196D475X035JE3	56289	
C22 Thru C25	Same as C13				
C26	Same as C21				
C27	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 200 V	1	8131A200Z5U103M	72982	
C28	Same as C4				
CR1	Diode	3	1N4449	80131	93332
CR2	Same as CR1				
CR3	Same as CR1				
CR4	Diode	1	1N4446	80131	93332
CR5	Diode	2	1N462A	80131	93332
CR6	Same as CR5				
CR7	Diode	2	MPD400	09213	
CR8	Same as CR7				
J1	Connector, Receptacle	1	1-87567-6	00779	
Q1	Transistor	1	2N3251	80131	04713
Q2	Transistor	1	2N2222A	80131	04713
R1	Resistor, Fixed, Composition: 10 kΩ, 5%, 1/4 W	4	RCR07G103JS	81349	01121
R2	Resistor, Fixed, Composition: 22 Ω, 5%, 1/2 W	1	RCR20G220JS	81349	01121
R3	Resistor, Fixed, Composition: 1.0 kΩ, 5%, 1/4 W	1	RCR07G102JS	81349	01121
R4	Resistor, Fixed, Composition: 3.9 kΩ, 5%, 1/4 W	1	RCR07G392JS	81349	01121
R5	Resistor, Fixed, Composition: 6.8 kΩ, 5%, 1/4 W	1	RCR07G682JS	81349	01121
R6	Resistor, Fixed, Composition: 12 kΩ, 5%, 1/4 W	1	RCR07G123JS	81349	01121
R7	Resistor, Fixed, Composition: 7.5 kΩ, 5%, 1/4 W	1	RCR07G752JS	81349	01121

REF DESIG PREFIX 232-A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R8	Resistor, Fixed, Composition: 20 kΩ, 5%, 1/4 W	1	RCR07G203JS	81349	01121
R9	Resistor, Fixed, Composition: 6.2 kΩ, 5%, 1/4 W	1	RCR07G622JS	81349	01121
R10	Resistor, Variable, Film: 1 kΩ, 10%, 1/2 W	1	62PAR1K	73138	
R11	Resistor, Fixed, Composition: 100 Ω, 5%, 1/4 W	1	RCR07G101JS	81349	01121
R12	Resistor, Fixed, Composition: 1.5 kΩ, 5%, 1/4 W	2	RCR07G152JS	81349	01121
R13	Same as R12				
R14	Resistor, Variable, Film: 2 kΩ, 10%, 1/2 W	1	62PAR2K	73138	
R15	Resistor, Fixed, Composition: 2.7 kΩ, 5%, 1/4 W	3	RCR07G272JS	81349	01121
R16	Resistor, Fixed, Composition: 51 kΩ, 5%, 1/4 W	1	RCR07G513JS	81349	01121
R17	Resistor, Fixed, Composition: 82 Ω, 5%, 1/4 W	1	RCR07G820JS	81349	01121
R18	Same as R1				
R19	Resistor, Fixed, Composition: 3.3 kΩ, 5%, 1/4 W	2	RCR07G332JS	81349	01121
R20	Same as R1				
R21	Same as R15				
R22	Same as R15				
R23	Same as R1				
R24	Same as R1				
R25	Resistor, Fixed, Composition: 820 kΩ, 5%, 1/4 W	1	RCR07G821JS	81349	01121
R26	Resistor, Variable, Film: 1 kΩ, 10%, 1/2 W	1	62PR1K	73138	
R27	Resistor, Fixed, Composition: 1.0 MΩ, 5%, 1/8 W	4	RCR05G105JS	81349	01121
R28 Thru R30	Same as R27				
R31	Resistor, Fixed, Composition: 120 Ω, 5%, 1/4 W	1	RCR07G121JS	81349	01121
R32	Resistor, Fixed, Composition: 10 kΩ, 5%, 1/8 W	4	RCR05G103JS	81349	01121
R33 Thru R35	Same as R32				
R36	Resistor, Fixed, Composition: 220 Ω, 5%, 1/4 W	1	RCR07G221JS	81349	01121
R37	Resistor, Fixed, Composition: 47 kΩ, 5%, 1/4 W	1	RCR07G473JS	81349	01121
R38	Same as R19				
U1	Integrated Circuit	1	P8085A	34649	
U2	Integrated Circuit	1	SN74LS125N	01295	
U3	Integrated Circuit	1	CD4013BE	02735	
U4	Integrated Circuit	1	SN74LS14N	01295	
U5	Integrated Circuit	1	MM74C14N	27014	
U6	Resistor, Network: 10 kΩ	1	764-1-R10K	73138	
U7	Integrated Circuit	1	SN74LS138N	01295	
U8	Integrated Circuit	1	CD4053BE	02735	
U9	Integrated Circuit	1	SN74LS241N	01295	
U10	Integrated Circuit	4	SN74LS273N	01295	
U11	Same as U10				

REF DESIG PREFIX 232-A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U12	Same as U10				
U13	Same as U10				
U14	Integrated Circuit	1	SN74LS240N	01295	
U15	Integrated Circuit	1	MC14050BCP	04713	
U16	Not Used				
U17	Integrated Circuit	2	747PC	07263	
U18	Same as U17				
U19	Integrated Circuit	1	MC1408L8	04713	
U20	Integrated Circuit	1	ADC0800PCN	27014	
U21	Integrated Circuit	1	SN74LS08N	01295	
U22	Integrated Circuit	1	NE555N	18324	
VR1	Diode, Zener: 3.3 V	1	1N746A	80131	04713
VR2	Diode, Zener: 12 V	1	1N759A	80131	04713
VR3	Diode, Zener: 5.1 V	2	1N751A	80131	04713
VR4	Same as VR3				
XV1	Socket, IC	1	US-2-40-110-G-B	18677	

1.10.3 TYPE 796037 ASYNCHRONOUS I/O BOARD REF DESIG PREFIX 232-A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C1	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 15 V	3	196D226X0015KE3	56289	
C2	Same as C1				
C3	Same as C1				
C4	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 100 V	5	8131M100-651-104M	72982	
C5 Thru C8	Same as C4				
J1	Connector, Receptacle	2	87567-6	00779	
J2	Same as J1				
J3	Connector, Receptacle	18	006-4800	98291	
J4 Thru J20	Same as J3				
P1	Connector, Plug	6	021-4802	98291	
P2 Thru P6	Same as P1				
R1	Resistor, Fixed, Composition: 100 Ω, 5%, 1/4 W	2	RCR07G101JS	81349	01121
R2	Same as R1				
R3	Resistor, Fixed, Composition: 3.3 k Ω, 5%, 1/8 W	2	RCR05G332JS	81349	01121
R4	Same as R3				
R5	Resistor, Fixed, Composition: 10 k Ω, 5%, 1/8 W	4	RCR05G103JS	81349	01121
R6	Same as R5				
R7	Same as R5				
R8	Same as R5				
S1	Switch, Dip: SPST	1	PIP-4	01686	
S2	Switch, Dip: SPST	1	PIP-8	01686	
U1	Integrated Circuit	1	P8251A	34649	
U2	Integrated Circuit	1	SN74LS273N	01295	
U3	Integrated Circuit	1	DM81LS96N	27014	
U4	Integrated Circuit	1	SN74LS138N	01295	
U5	Integrated Circuit	1	C0M5046P	53848	
U6	Integrated Circuit	1	SN74LS04N	01295	
U7	Integrated Circuit	2	9616PC	07263	
U8	Same as U7				
U9	Integrated Circuit	2	9617PC	07263	
U10	Same as U9				
U11	Resistor Network: 10 kΩ	1	764-1-R10K	73138	
VR1	Diode, Zener: 12 V	2	1N759A	80131	04713
VR2	Same as VR1				
XU1	Socket, IC	1	US-2-28-110-G-B	18677	
Y1	Crystal Quartz: 5.0688 MHz	1	91805-4	14632	

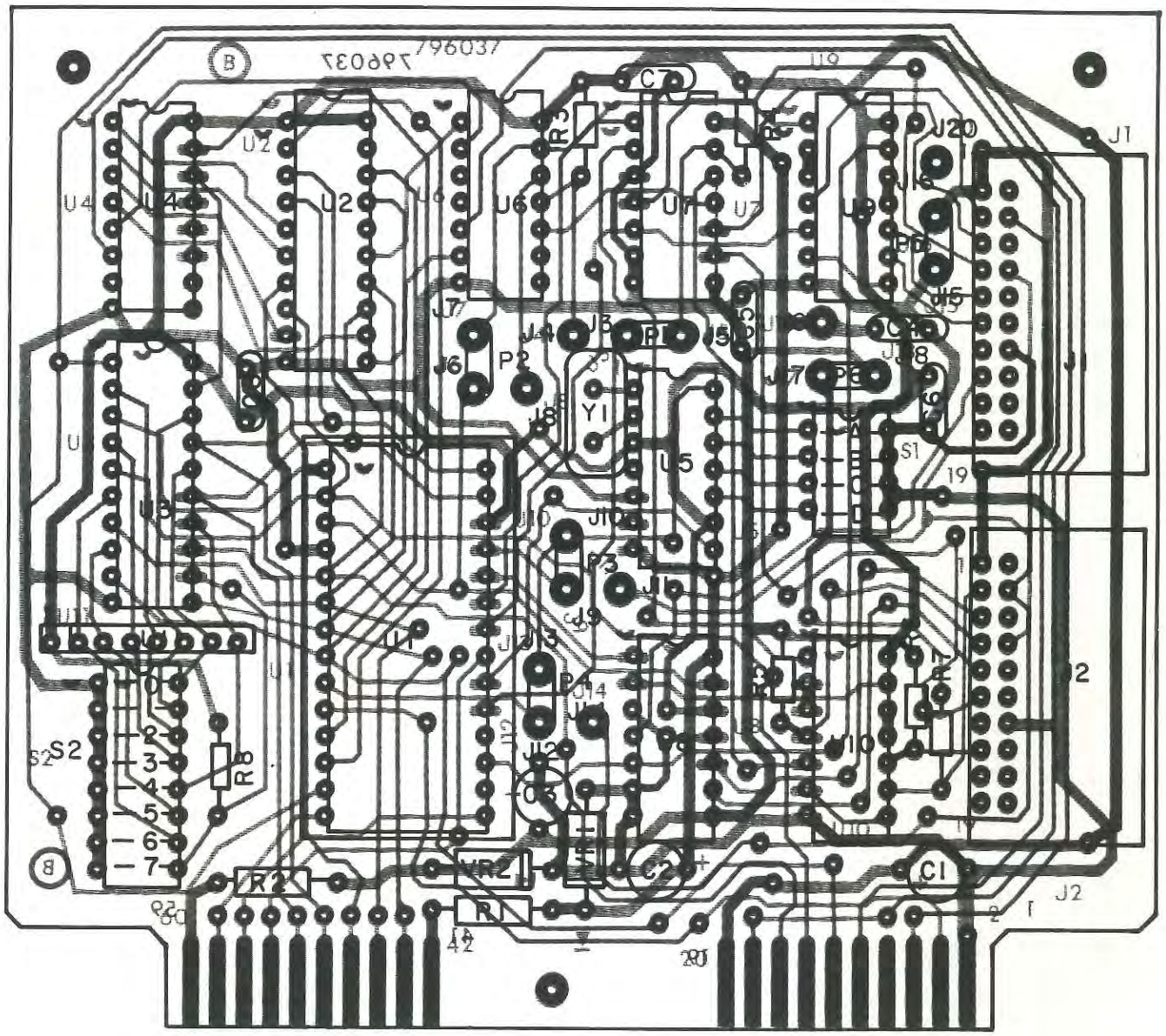


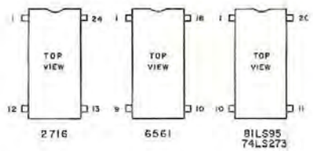
Figure 1-21. Type 796037 Asynchronous I/O Board, Location of Components

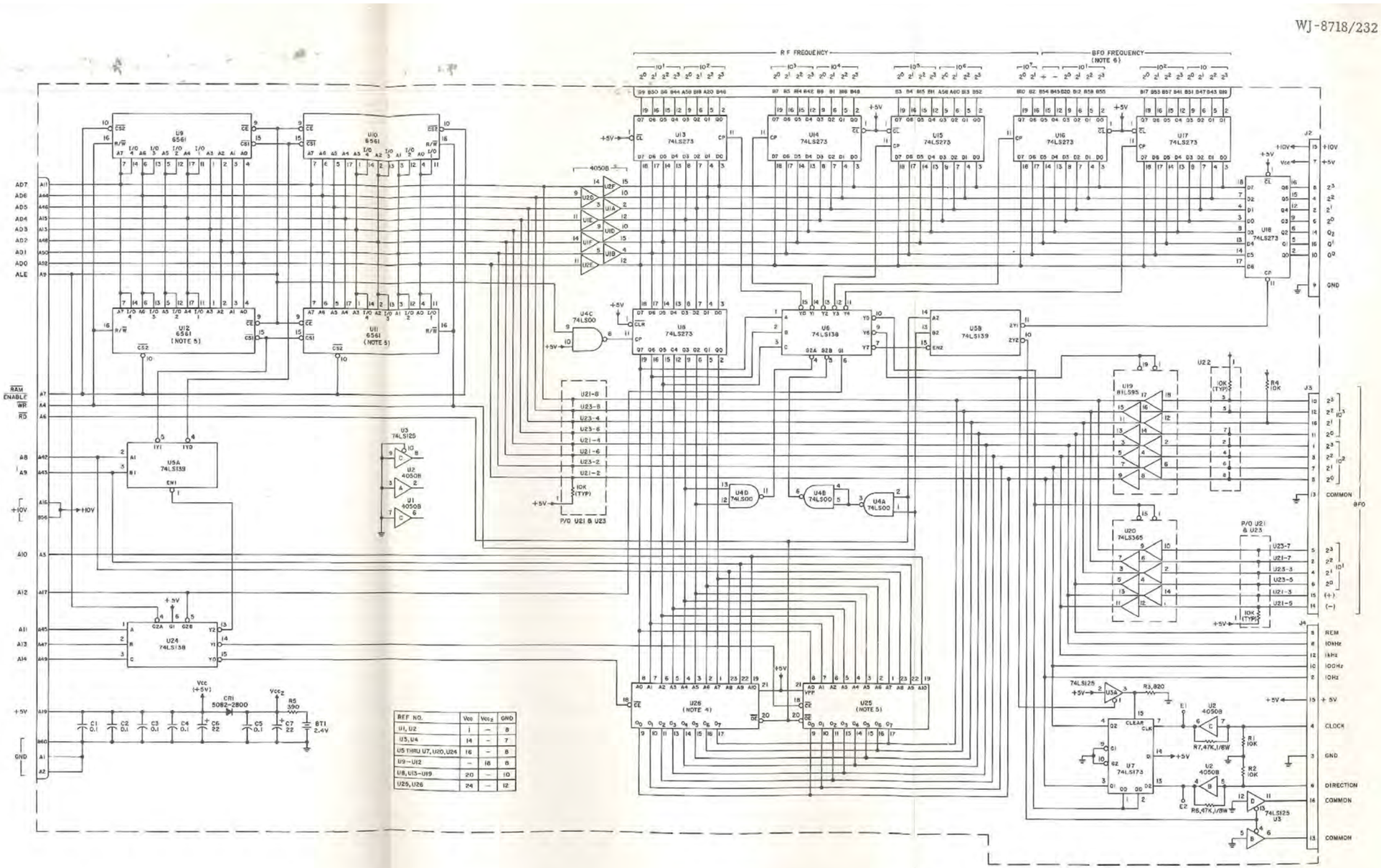
TABLE A

TYPE	U25
796029-1	841034
796029-2	841036
796029-3	841039

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
2. FOR Vcc & GND SEE TABULATION BLOCK.
3. FOR IC PIN ARRANGEMENT SEE DETAIL A.
4. DIFFERENCE BETWEEN TYPES IS SHOWN IN TABLE A.
5. U25, U11 & U12 ARE FUTURE USE, NOT USED AT THIS TIME
6. BFO FREQUENCY 10 WHEN USED IN 8718/232-3 IS NONCLAMENTURED AS RF TUNING 10⁰.

DETAIL A





REF NO.	Vcc	Vcc_2	GND
U1, U2	1	–	8
U3, U4	14	–	7
U5 THRU U7, U20, U24	16	–	8
U9–U12	–	18	8
U8, U13–U19	20	–	10
U25, U26	24	–	12

Figure 1-22. Type 796029-1 Synthesizer Interface Board (232-A1), Schematic Diagram 680014

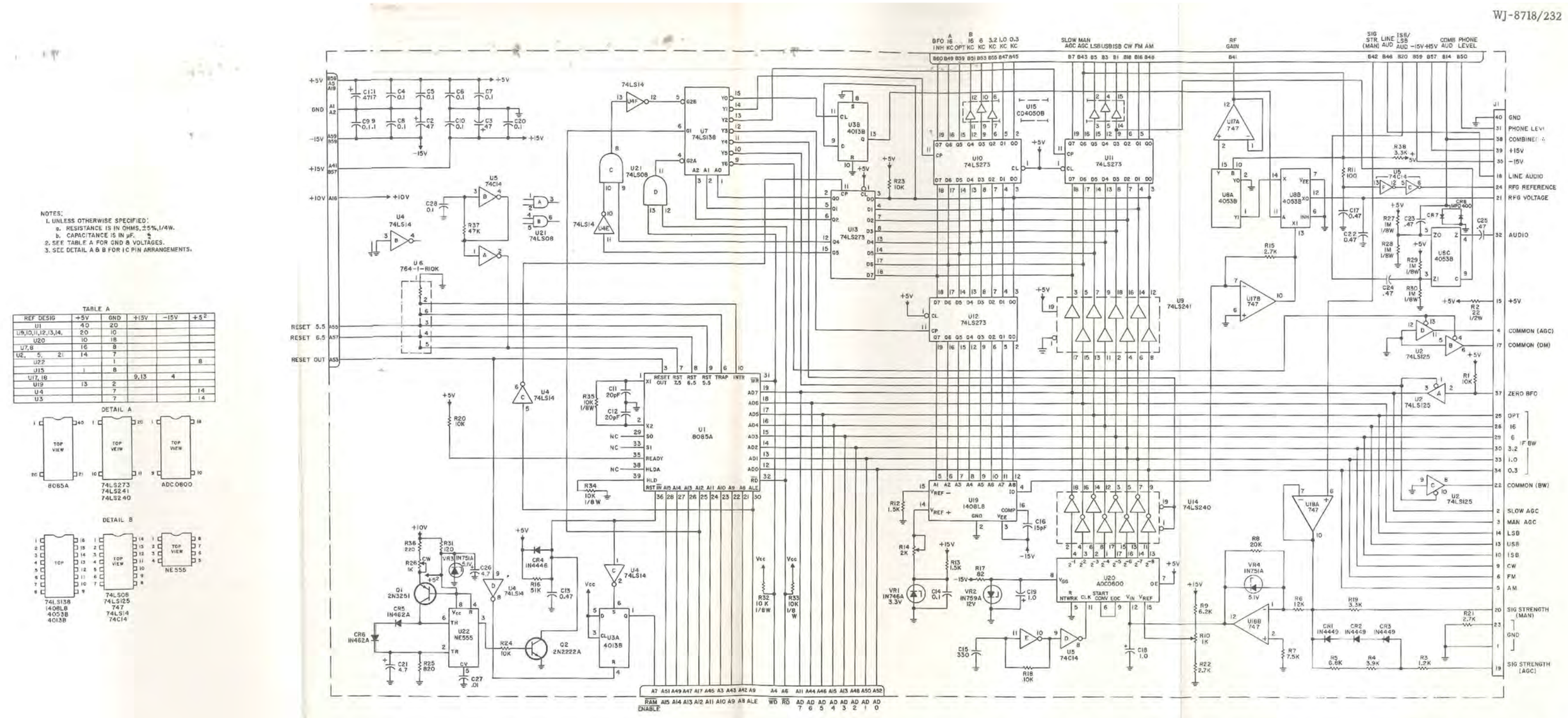


Figure 1-23. Type 796032 IF Interface Board (232-A2), Schematic Diagram 680016

TABLE A

D C B A	BAUD RATE
0 0 0 0	50
0 0 0 1	75
0 0 1 0	110
0 0 1 1	134.5
0 1 0 0	150
0 1 0 1	300
0 1 1 0	600
0 1 1 1	1200
1 0 0 0	1800
1 0 0 1	2000
1 0 1 0	2400
1 0 1 1	3600
1 1 0 0	4800
1 1 0 1	7200
1 1 1 0	9600
1 1 1 1	19,200

1=OPEN

TABLE B

	Vcc	GND	+12V	−12V
U1	26	4	—	—
U2	20	10	—	—
U3, U4	16	8	—	—
U5	3	5	7	—
U6, U9, U10	14	7	—	—
U7, U8	—	7	14	8

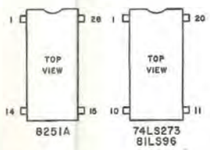
TABLE C

UNIT ADDRESS							
S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
MASTER SLAVE	PARITY EN	EVEN PARITY	2^4	2^3	2^2	2^1	2^0

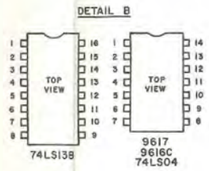
1= CLOSED

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN μF.
2. SEE TABLE B FOR Vcc AND GND.
3. SEE DETAILS A & B FOR I/C PIN CONFIGURATIONS.
4. P1, P2 AND P6 ARE SHOWN FOR RS-232 CONFIGURATION. ALTERNATE CONNECTIONS ARE FOR MIL-188C.
5. P3 AND P4 ARE SHOWN FOR ASYNCHRONOUS OPERATION. ALTERNATE CONNECTIONS ARE FOR SYNCHRONOUS OPERATION.
6. BAUD RATE SELECTION IS SHOWN IN TABLE A.
7. ADDRESS SELECTION AND PARITY SELECTION ARE SHOWN IN TABLE C.

DETAIL A



DETAIL B



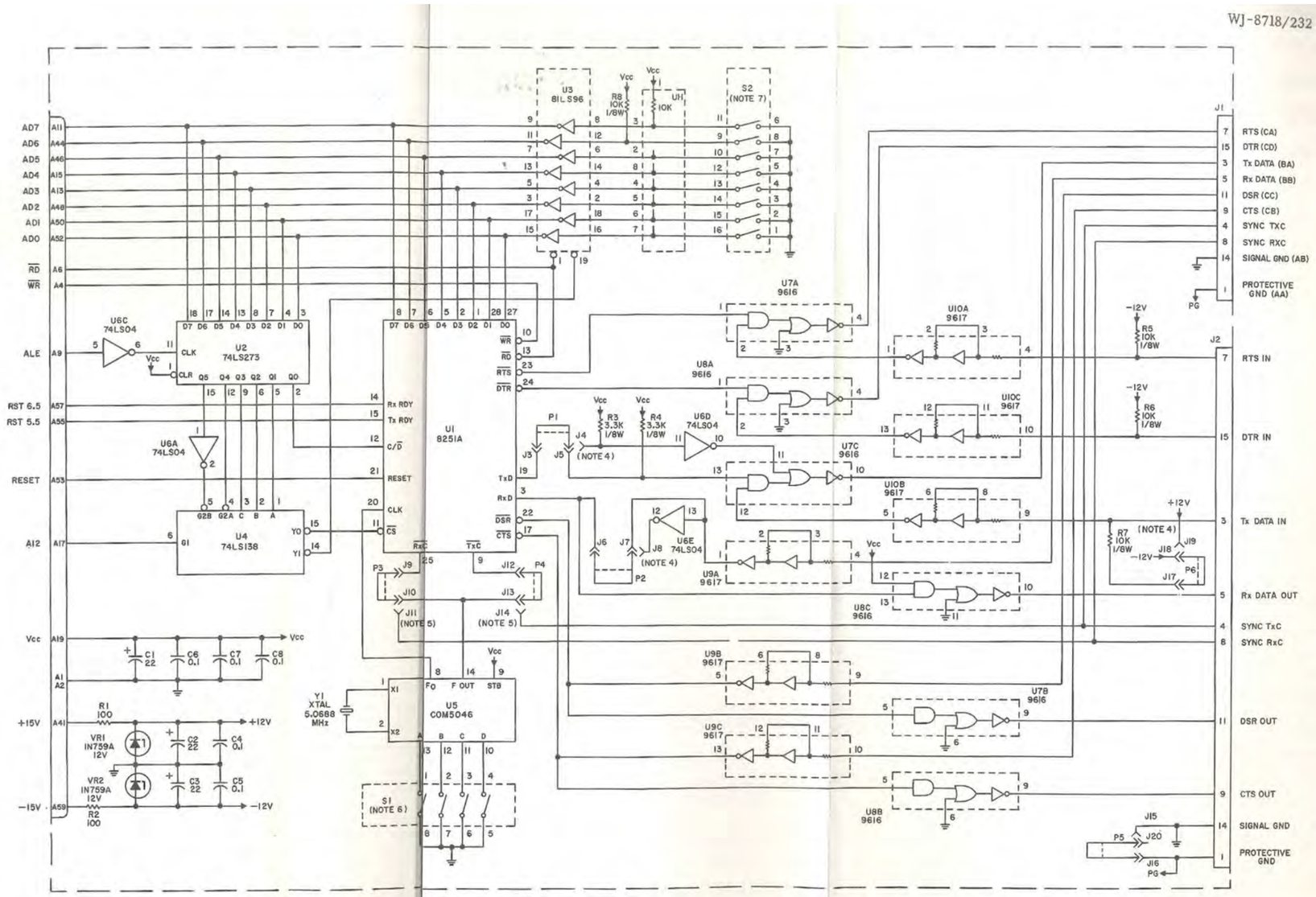


Figure 1-24. Type 796037 Asynchronous I/O Board (232-A3), Schematic Diagram 580023

NOTES
1. PHANTOM LINES INDICATE PRE-EXISTING MODULES.
2. 232-A1 REPLACES A6A1, 232-A2 REPLACES A6A2 OF MAIN FRAME WHEN 8718/232 OPTION IS IMPLEMENTED.
3. 232-P1, 232-P2 & 232-P3 OF 232-W1 ARE WIRED PIN FOR PIN.
4. DIFFERENCE BETWEEN UNITS IS SHOWN IN TABLE A.

TABLE A

UNIT	232-A1
8718/232	796029-1
8718/232-4	796029-4

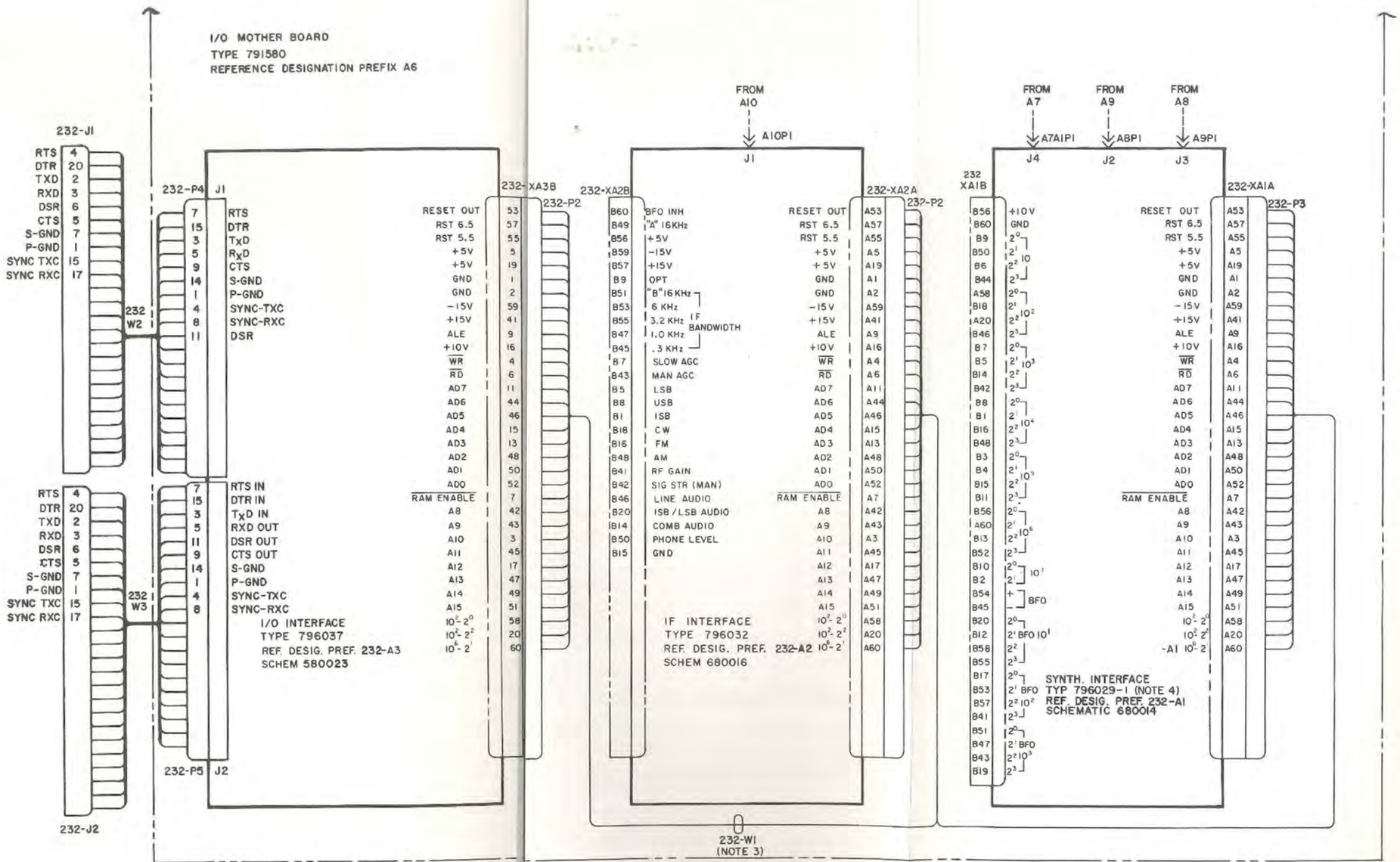


Figure 1-25. WJ-8718/232 Option Schematic Diagram 480098